MASTER CLASS April 8, 2026

Leading the Future of Logic with Materials-Enabled Scaling

APPLIED MATERIALS

Forward Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our capital allocation and cash deployment strategies, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic, political and industry conditions, including changes in interest rates and prices for goods and services; the implementation of additional export regulations and license requirements and their interpretation, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies and our ability to obtain licenses or authorizations on a timely basis, if at all; imposition of new or increases in tariffs and any retaliatory measures, including their impact on demand for our products and services; our ability to effectively mitigate the impact of tariffs; the effects of geopolitical turmoil or conflicts; demand for semiconductor chips and electronic devices; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; cybersecurity incidents affecting our information systems or information contained in them, or affecting our operations, suppliers, customers or vendors; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the effects of regional or global health epidemics; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our filings with the Securities and Exchange Commission, including our most recent Forms 10-K, 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

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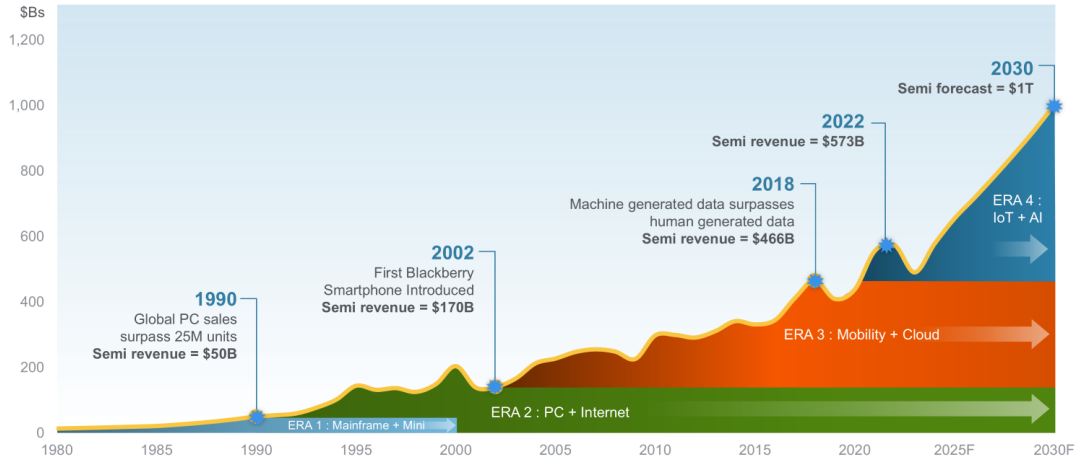
Welcome

Michael Sullivan
Corporate Vice President
Head of Investor Relations

APPLIED MATERIALS™

Prior View of Semi and WFE Markets

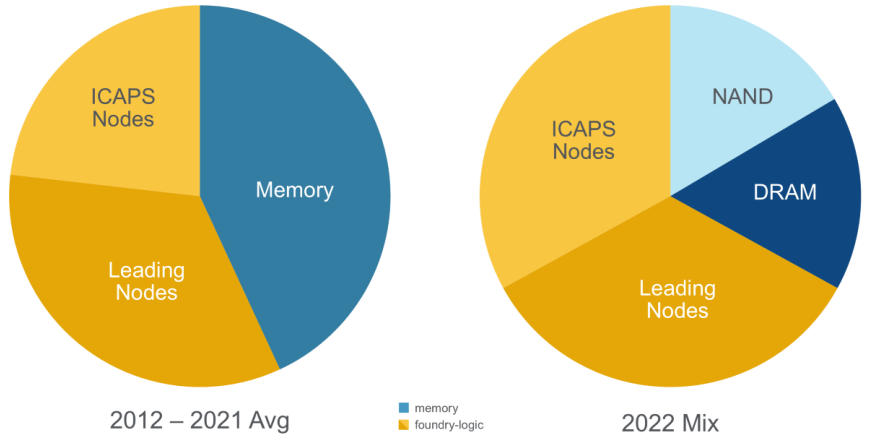
Our Semiconductor Industry Market Thesis



IoT + AI Era is the 4th and Biggest Age of Computing

Source 2030 forecast: TechInsights, McKinsey & Company, SEMI. Source Historical data: SIA, TechInsights, Applied Materials.

Expect Long-Term WFE to be Balanced: ICAPS, Leading, Memory



Long-term mix expected to be similar

Source: Gartner, TechInsights, Applied estimates. Leading nodes refers to 3nm, 5nm and 7nm.

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AI Accelerating Semiconductor Demand

NOW:
AI Intelligent Cloud

FUTURE:
AI Intelligence Everywhere!

Semiconductor industry revenues can potentially reach

$1T

this year

Source: SIA, Applied Materials

WFE Market Outlook

FASTEST GROWING AREAS OF THE MARKET

	INFLECTIONS
Leading-Edge Foundry/Logic	Gate-all-around transistors Backside power delivery
DRAM	$4F^2$ 3D DRAM
Advanced Packaging	High-bandwidth memory (HBM) Hybrid bonding Panel substrates

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#1 Process Equipment Company in All Three Markets

SLOWER GROWING AREAS

NAND	Increased layers Technology transitions
ICAPS	Compound semi (SiC, GaN) Photonics

ICAPS = IoT, Communications, Auto, Power, Sensors; represents nodes 10nm and larger

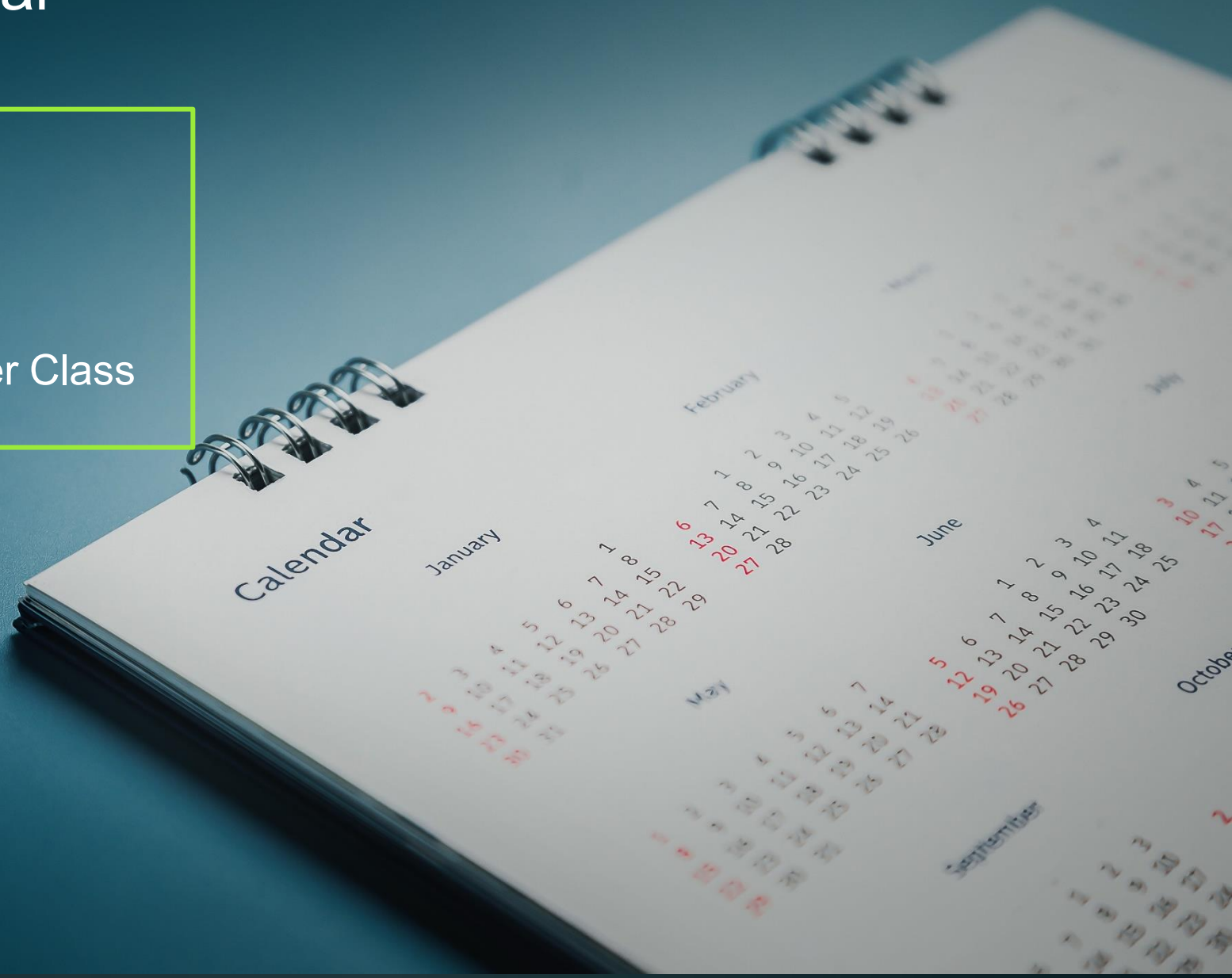
Inflection-Focused Calendar

APRIL 8 | 9AM PT
Logic Master Class
Webcast

JUNE 25 | 9AM PT
DRAM and Advanced Packaging Master Class
Webcast

OCTOBER 12
Investor Open House at the New EPIC Center Silicon Valley
Sunnyvale, CA

OCTOBER 13
Investor Breakfast
San Francisco, CA | Webcast



AGENDA

Mike Sullivan
Welcome and Introduction

Kevin Moraes, Ph.D.
Innovation and Technology Strategy

Bala Haran, Ph.D.
Logic Transistor

Zhebo Chen, Ph.D.
Logic Wiring

Q&A
Kevin, Bala, Zhebo, Mike

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Innovation and Technology Strategy

Kevin Moraes, Ph.D.
Corporate Vice President
Strategy and Marketing
Semiconductor Products Group

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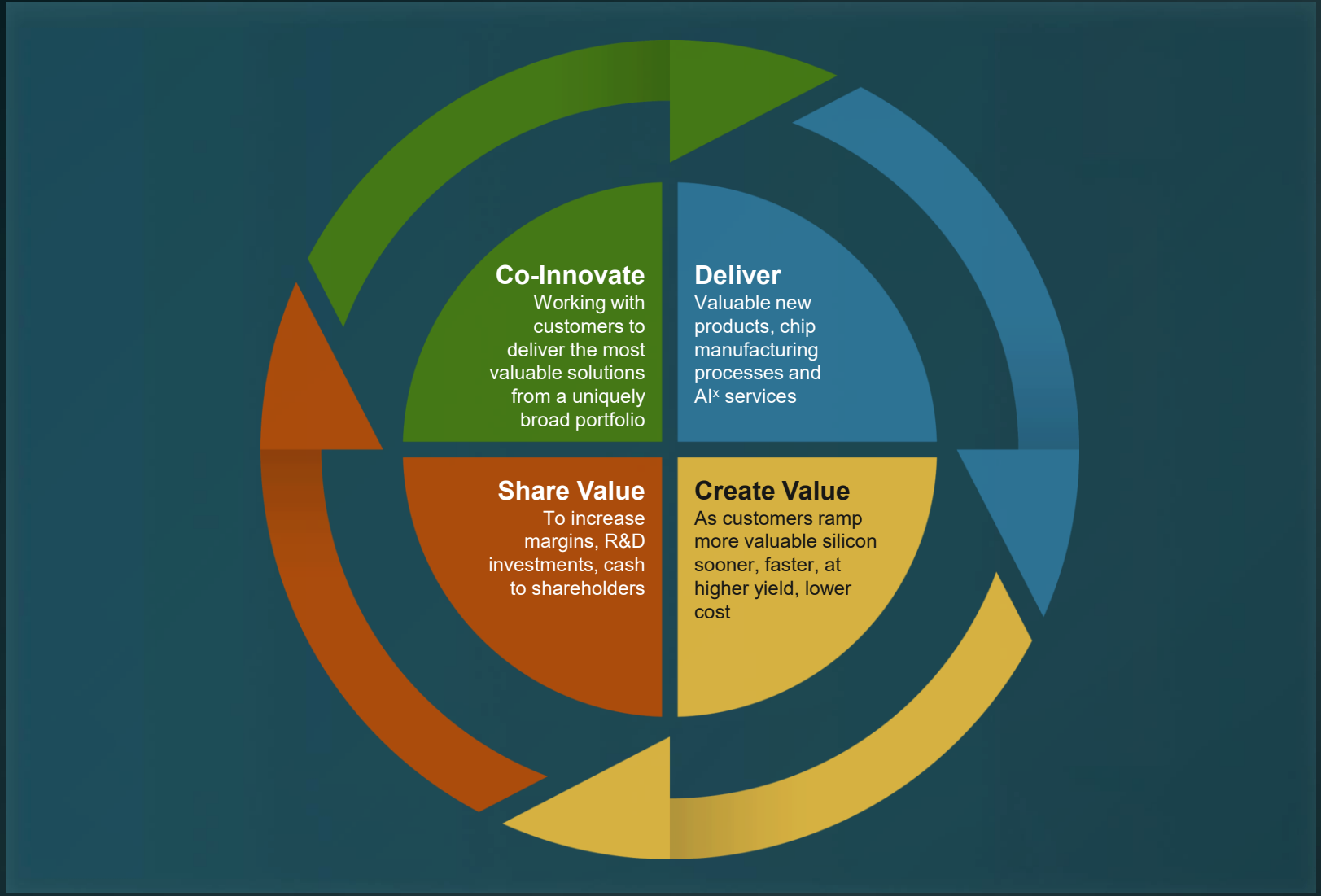
Inflection-Focused Innovation



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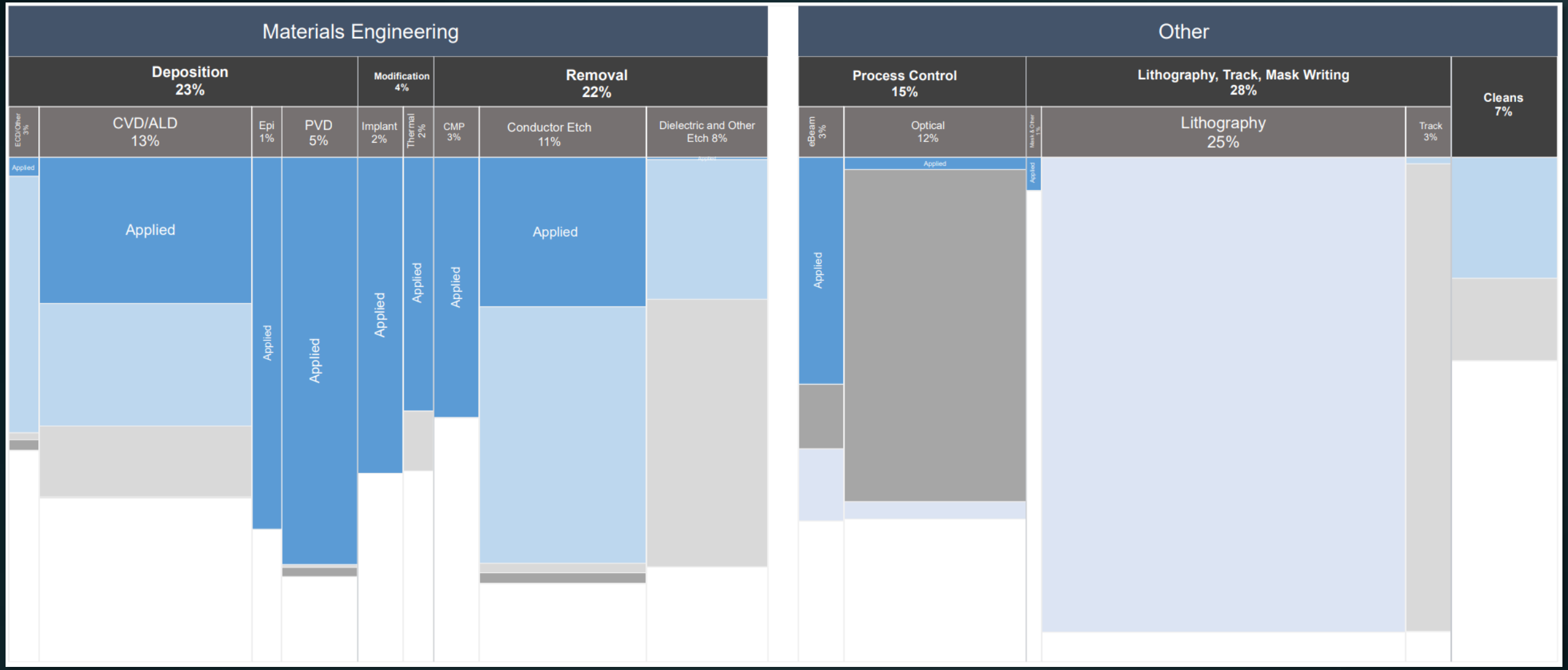
2025 WFE ($115B) by Technology – Materials Engineering ~50%



Source: TechInsights, April 2026. Wafer Fab Equipment (WFE) includes front-end fab equipment and excludes "Other WFE" of $4.2 billion.

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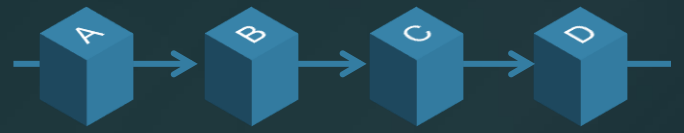
Broad Capabilities Delivered as Unique Connected Solutions

	Applied		Competitors			
ALD	✓	✓			✓	✓
Bonding	partner					✓
Cleans	partner				✓	✓
#1 CMP	✓					
#1 CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
#1 Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace	partner					✓
#1 Implant	✓					
Lithography	partner		✓			
M&I (optical)	✓			✓		
#1 M&I (e-beam)	✓		✓	✓		
#1 PVD	✓			✓		
#1 Thermal	✓					✓
Track						✓

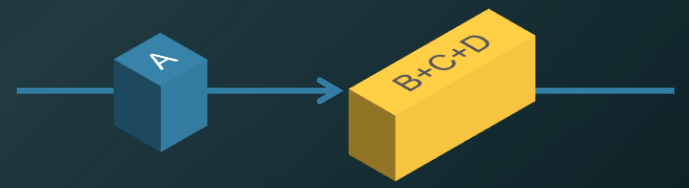
UNIQUE COMBINATIONS

Unit Process Tools



Co-optimized Solutions

Integrated Materials Solutions (IMS™)



Key Levers for Energy Efficient Compute

Threshold Voltage

Resistance

Capacitance

Variability

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Logic Transistor

Bala Haran, Ph.D.
Corporate Vice President
Integrated Materials Solutions
Semiconductor Products Group

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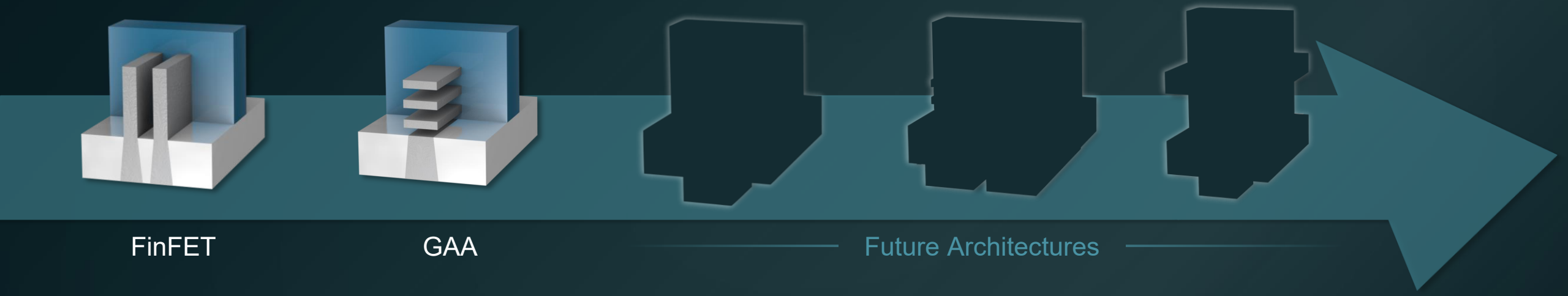
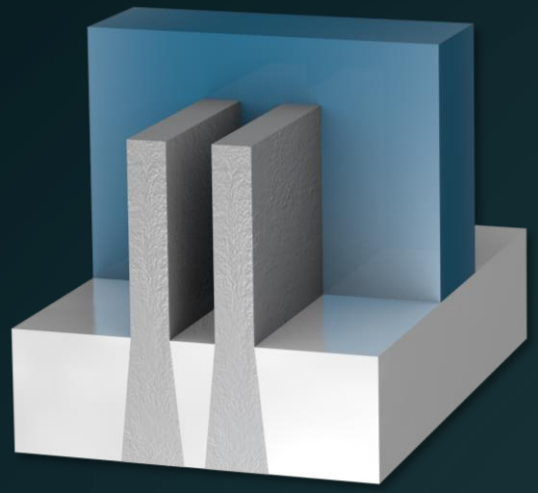
Transistor Evolution and Roadmap



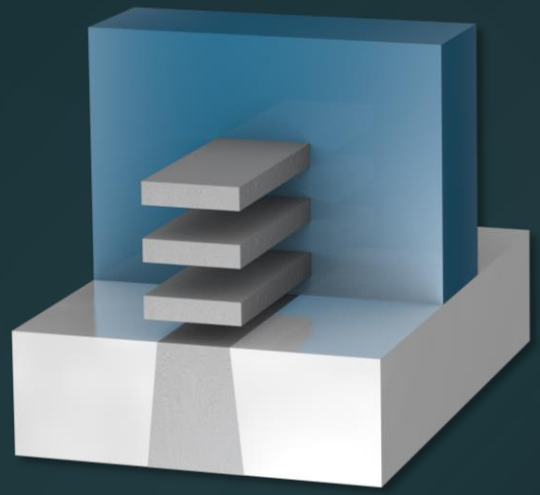
FinFET : fin field effect transistor
GAA: gate-all-around

FinFET → GAA: Improved Performance-Per-Watt

FinFET



GAA

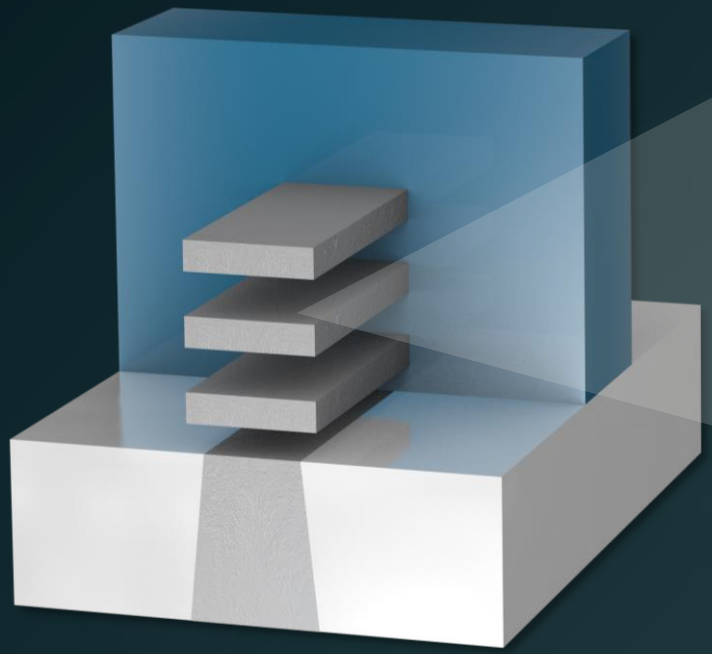


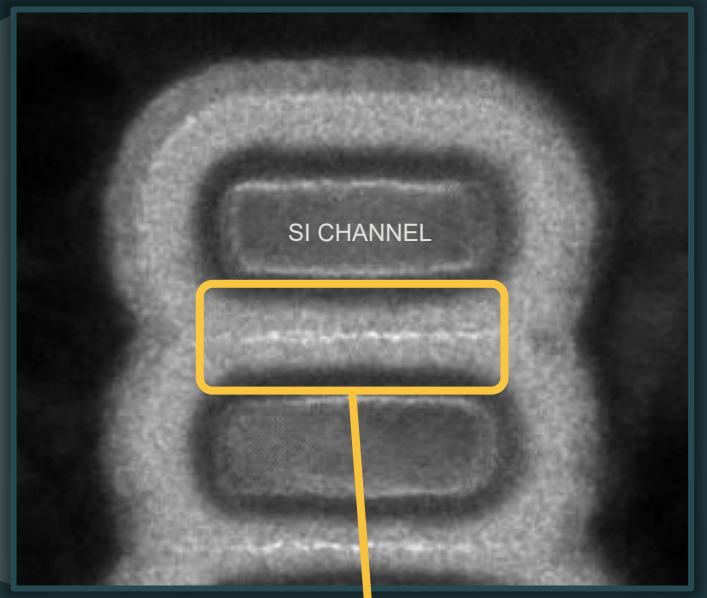
	FinFET	GAA
Channels	Vertical Fins	Stacked Horizontal Nanosheets
Gate Control	3 Sides	4 Sides
Complexity	Moderate	High

- ⬆ 20% Area Density
- ⬆ 20% Performance
- ⬇ 30% Power

FinFET : fin field effect transistor
GAA: gate-all-around

Logic Gate-All-Around Transistor Formation: High Process Complexity



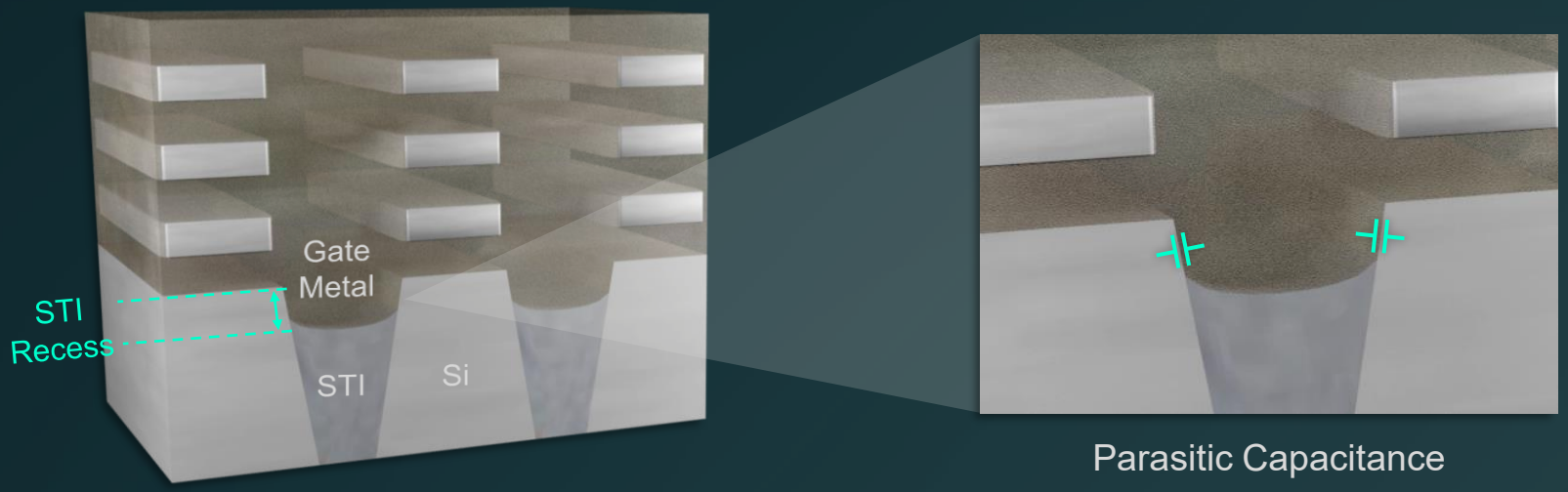


>500 steps
for GAA transistor

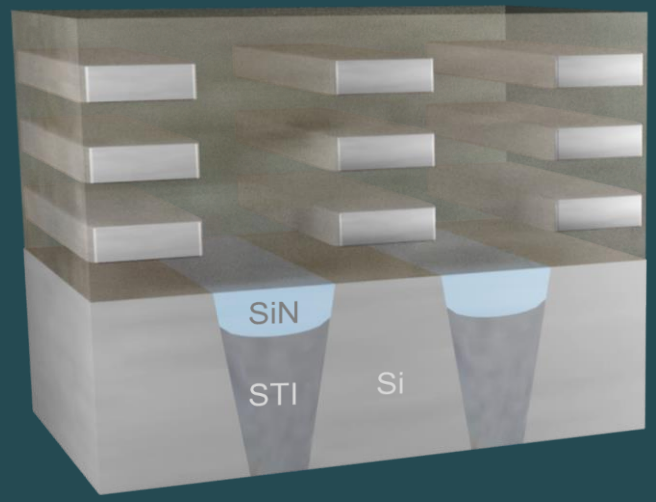
In just ~10nm between nanosheet channels

>5	1-2nm	1Å
distinct materials	per layer of material	precision required

Shallow Trench Isolation (STI) | Integrity

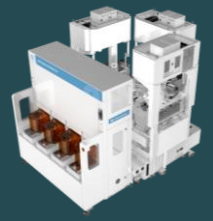


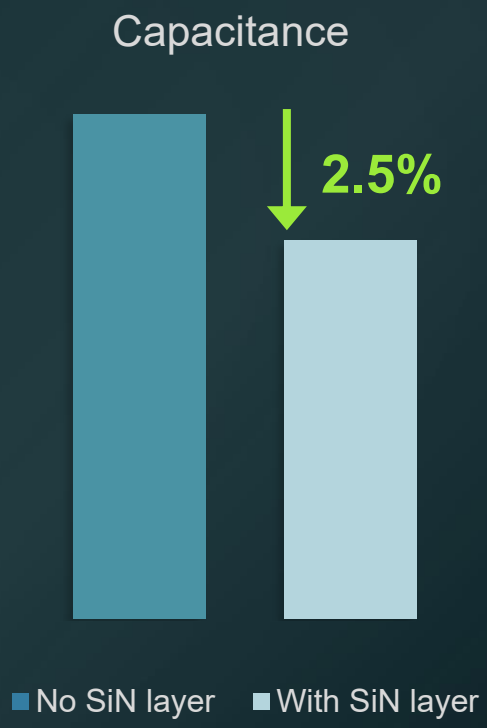
Parasitic Capacitance



Sym3™ Z Magnum™ Etch
Producer™ Selectra™ Etch

Producer™ Precision™ Selective Nitride PECVD

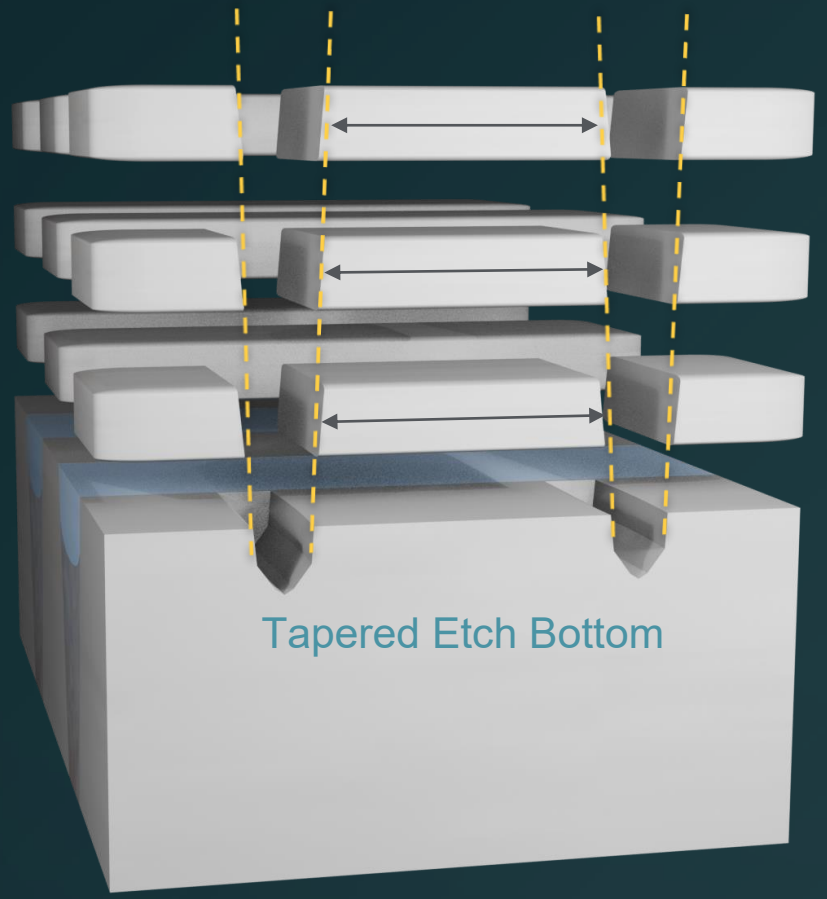




Creating Source/Drain | Etch

Challenge

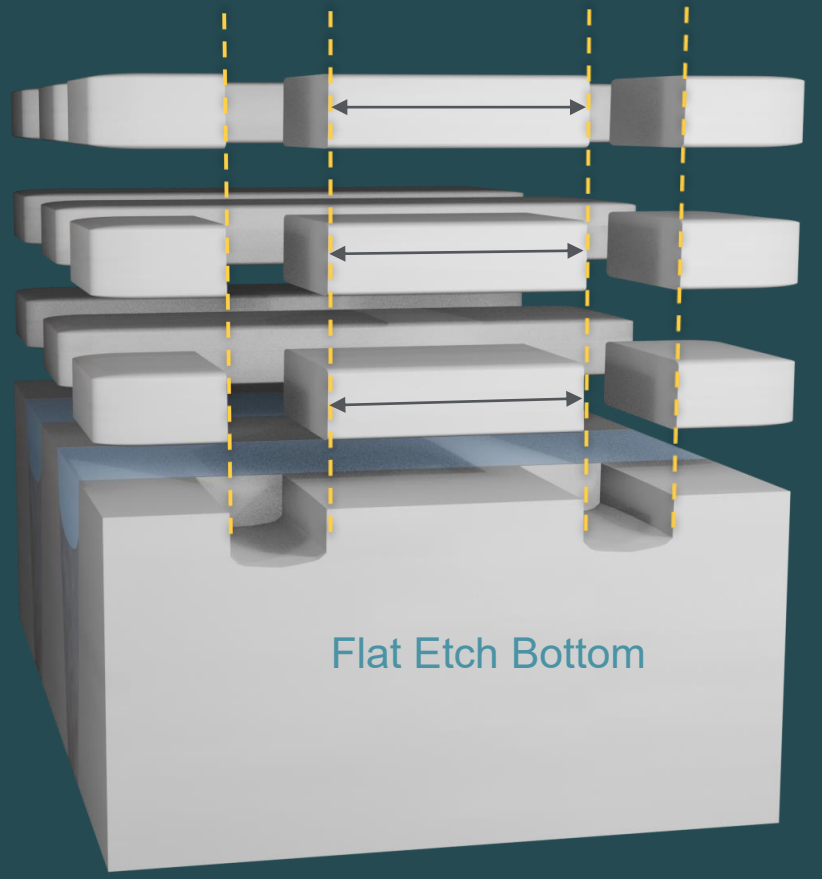
Tapered Etch Profile



Variable Gate Lengths

Tapered Etch Bottom

Vertical Etch Profile Control



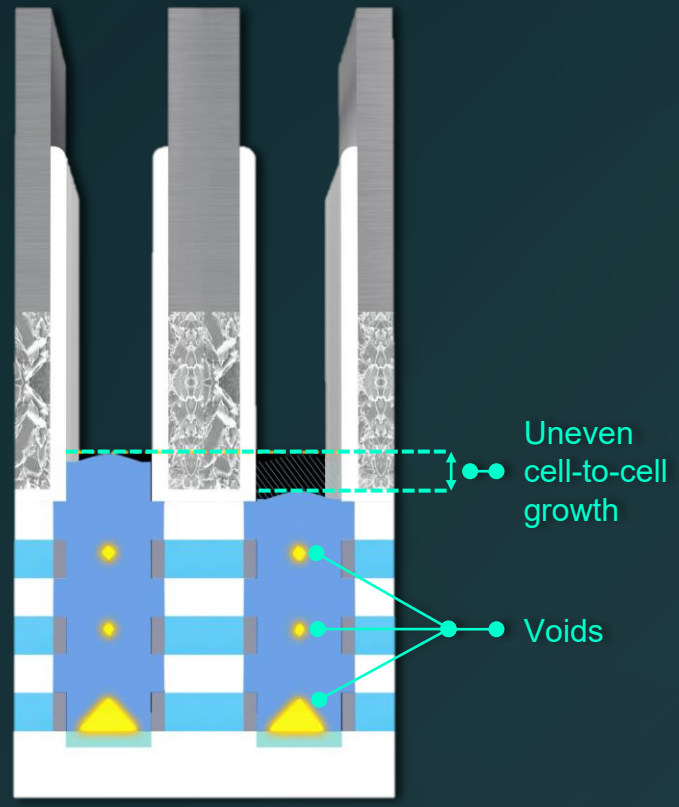
Uniform Gate Lengths

Flat Etch Bottom

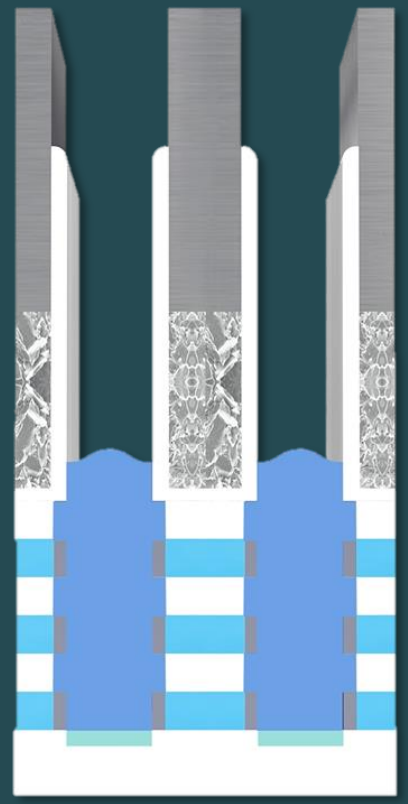
Sym3™ Z Magnum™ Etch with Pulsed Voltage Technology 2

Creating Source/Drain | Epitaxy

Challenge



Void-Free Uniform Growth

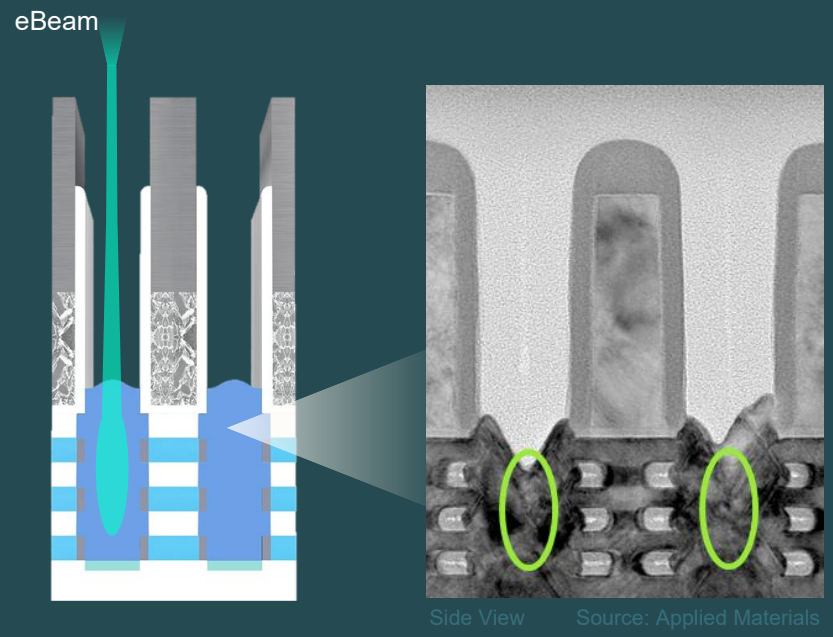


- Unique low chamber volume
- Tight control over chamber chemistry
- High-quality films with tailored chemistries for different transistors

Centura™ Xtera™ Epi

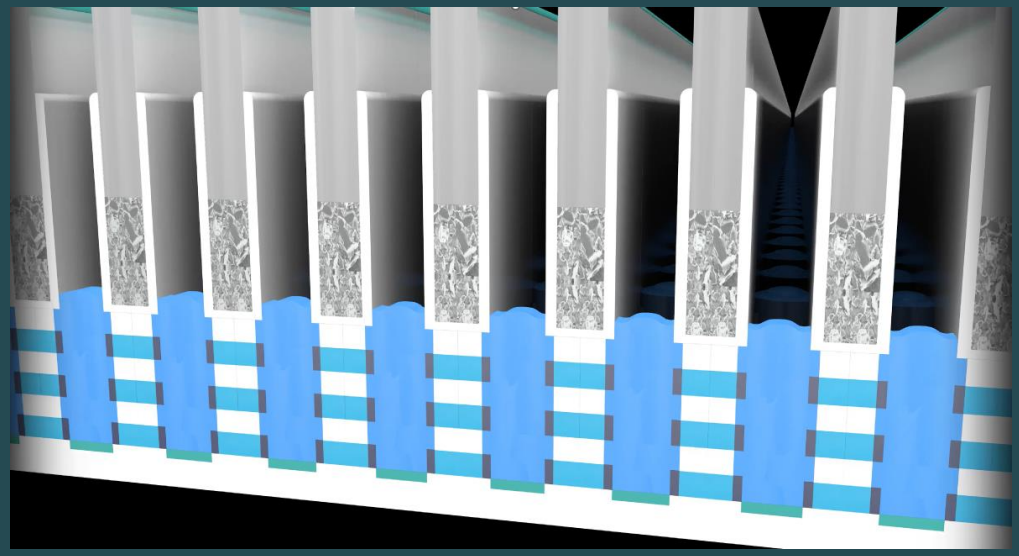
Creating Source/Drain | Process Co-Optimization with Metrology

PROVision™ 10 eBeam Metrology



High-resolution imaging inside device

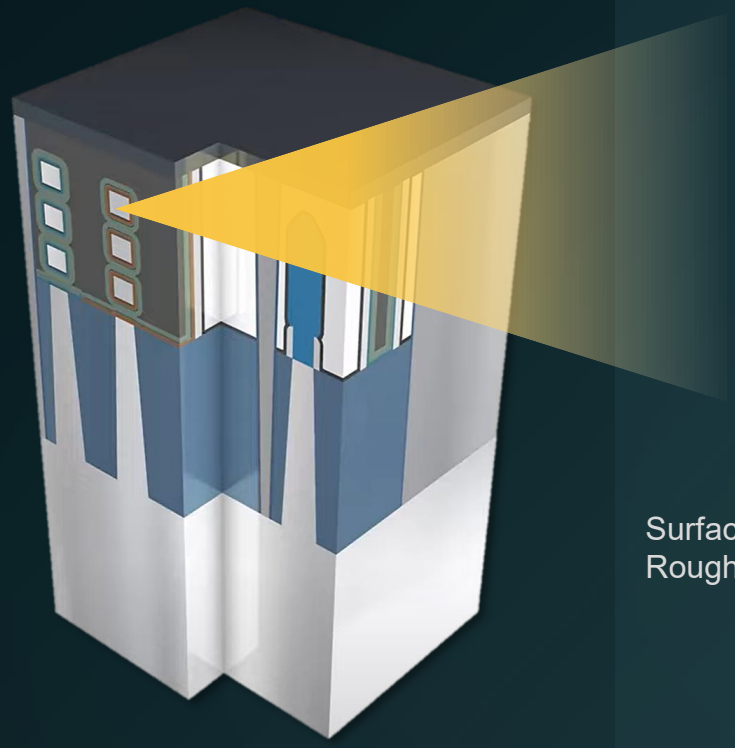
Co-optimization for Void-free and Uniform Cell Fill



40% improvement in cell-to-cell variation

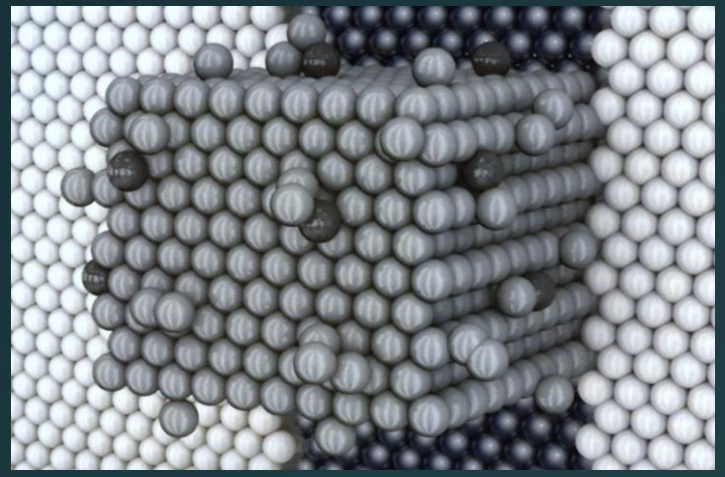
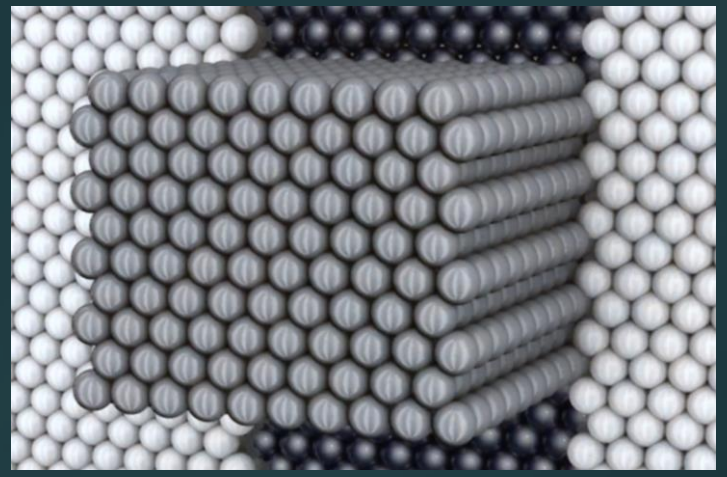
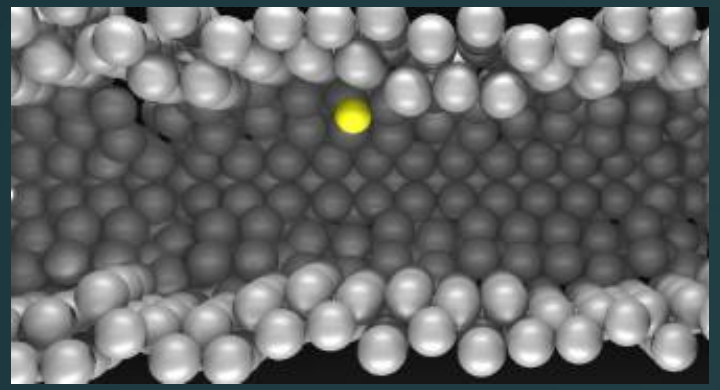
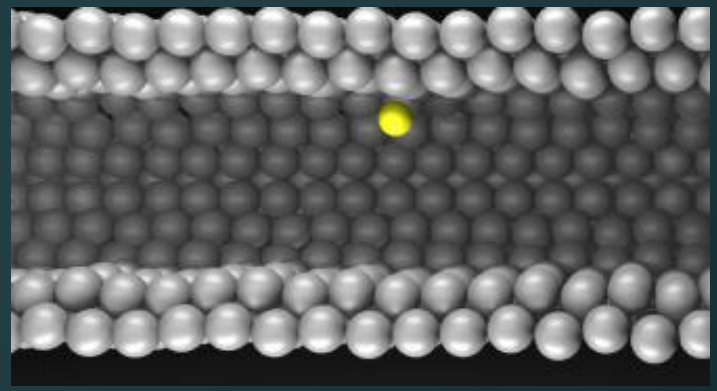
PROVision™ 10 eBeam Metrology
Centura™ Xtera™ Epi

Silicon Nanosheet Channel | Surface Treatment

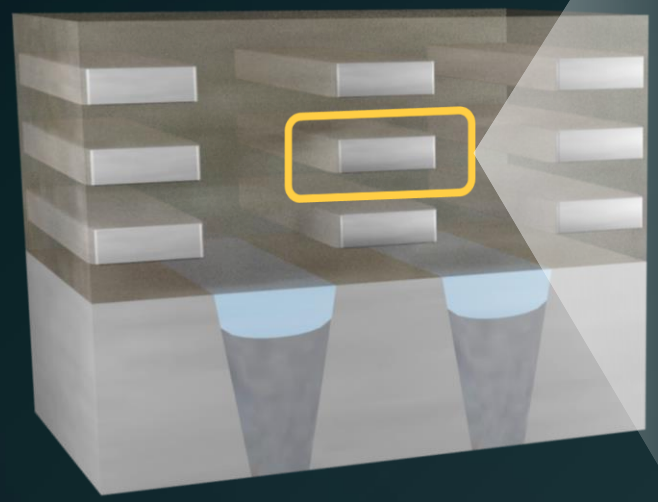


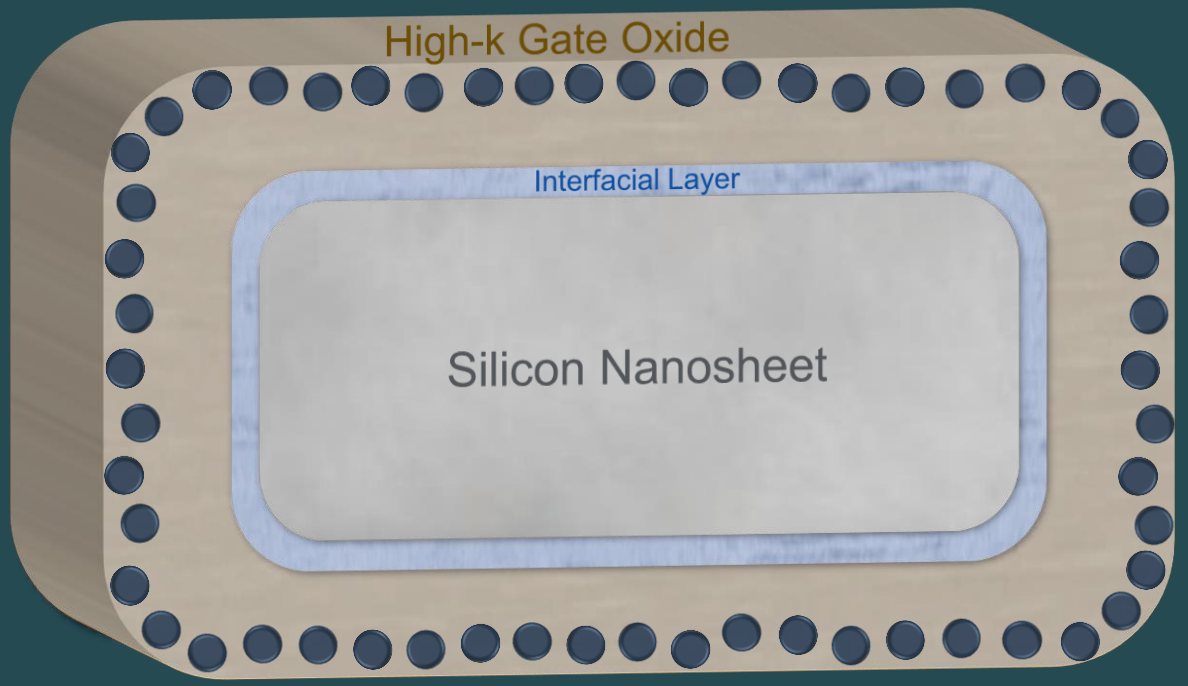
GAA Transistor

Producer™ Viva™ Radical Treatment

	Before Viva™	After Viva™
		
Surface Roughness		
Transistor Speed		

Gate Stack | High-k Gate Oxide Densification



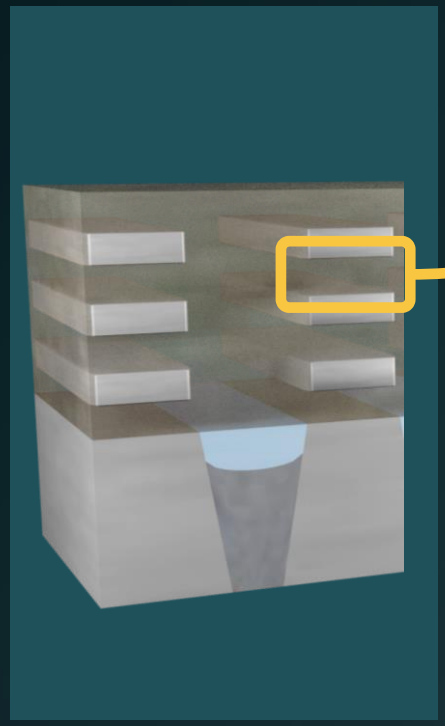


Centura™ DPN HD Treatment

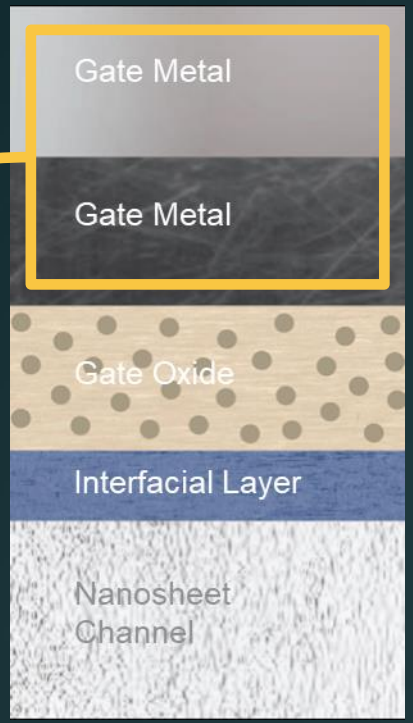
- Decoupled plasma nitride (DPN) chamber conformally introduces nitrogen
- Post-nitridation anneal strengthens nitrogen bonding with hafnium oxide

Gate Stack | Gate Metals

1
Gate Stack

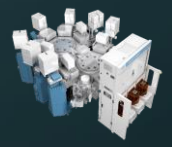


2
Gate Metals

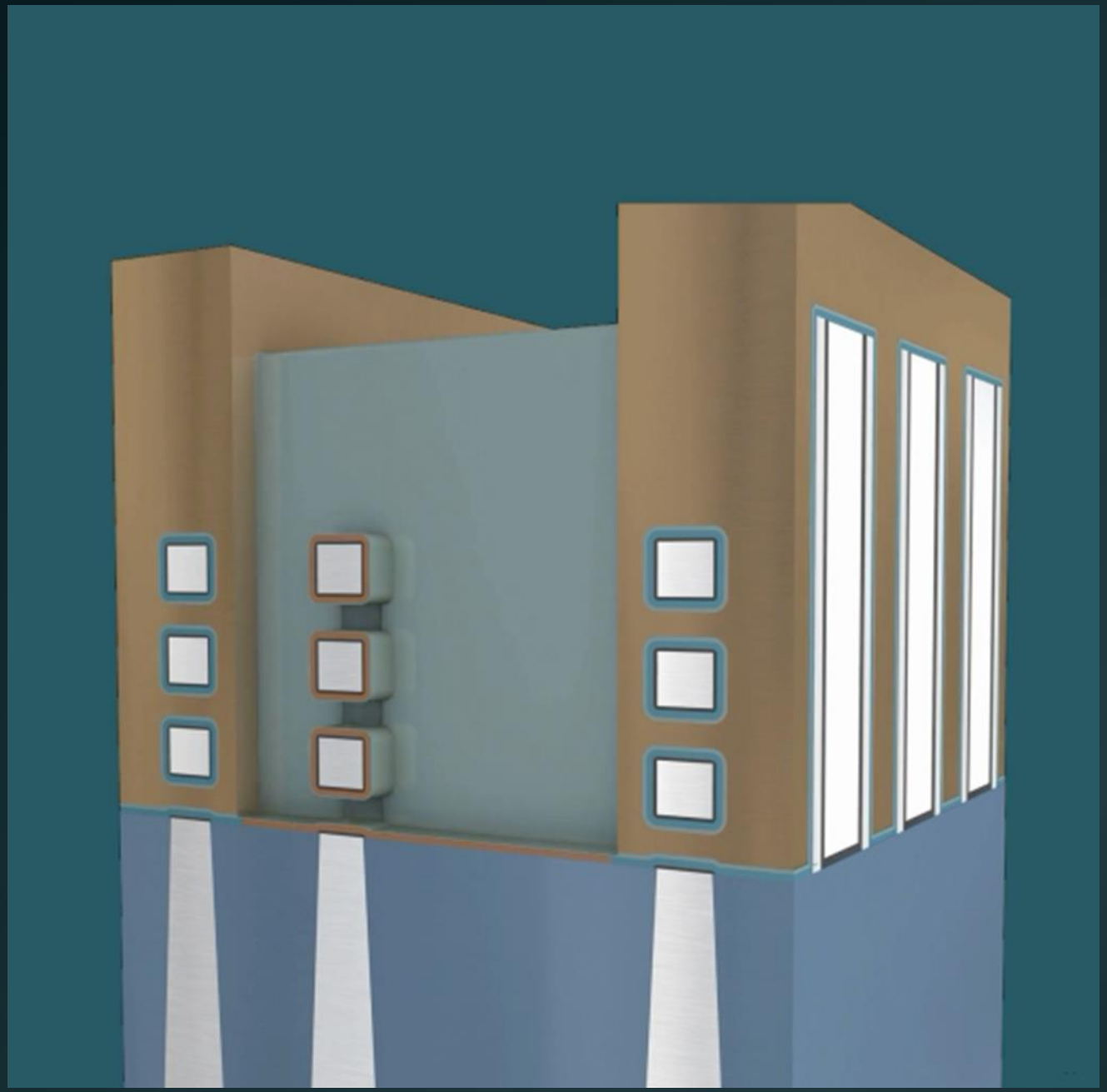


3
Transistor Behavior

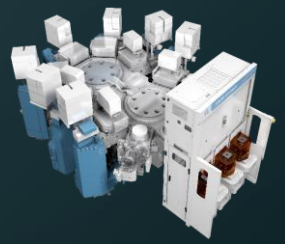
Endura™ Trillium™ ALD



APPLIED MATERIALS

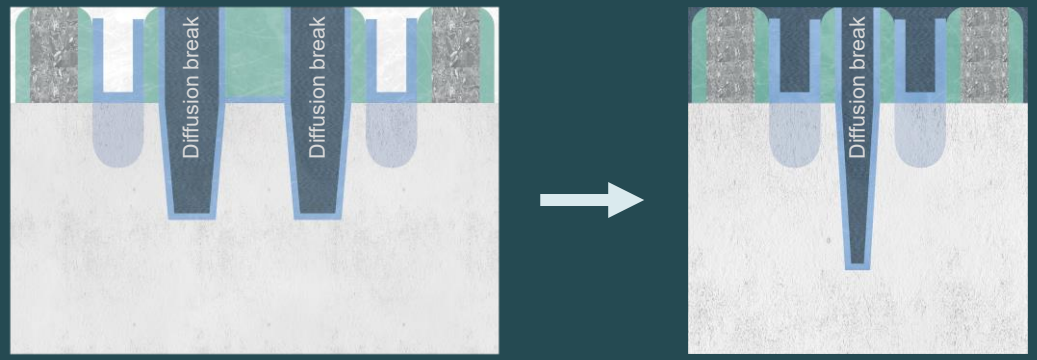


Advanced X-ray Metrology System
Endura™ Trillium™ ALD

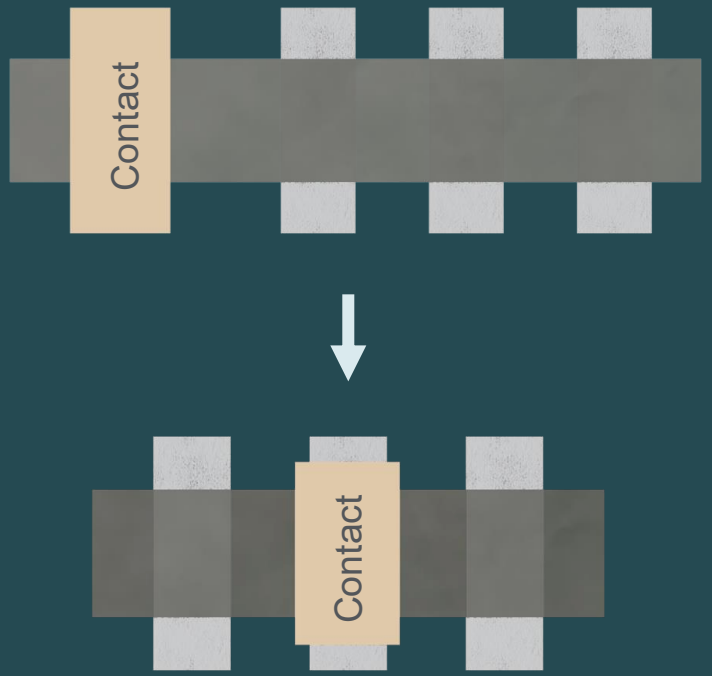


Cell Area Reduction Through DTCO

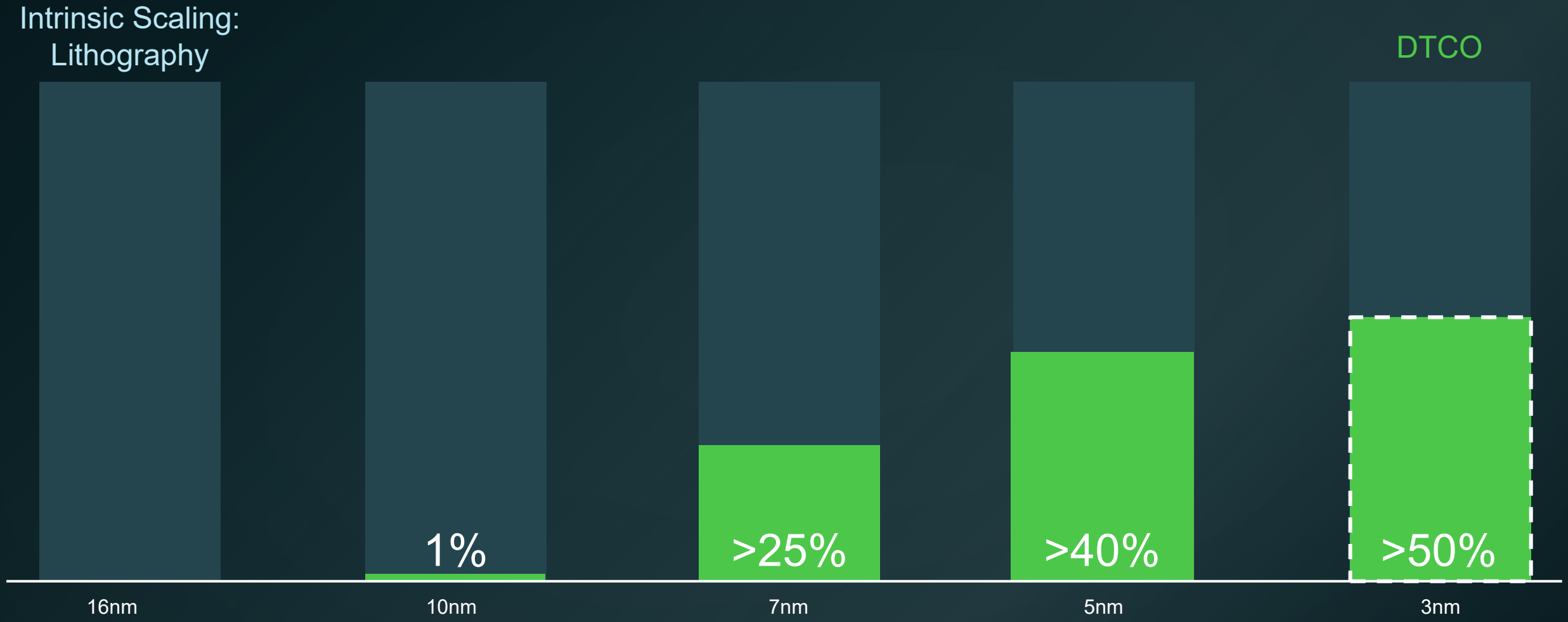
Single Diffusion Break



Contact Over Gate



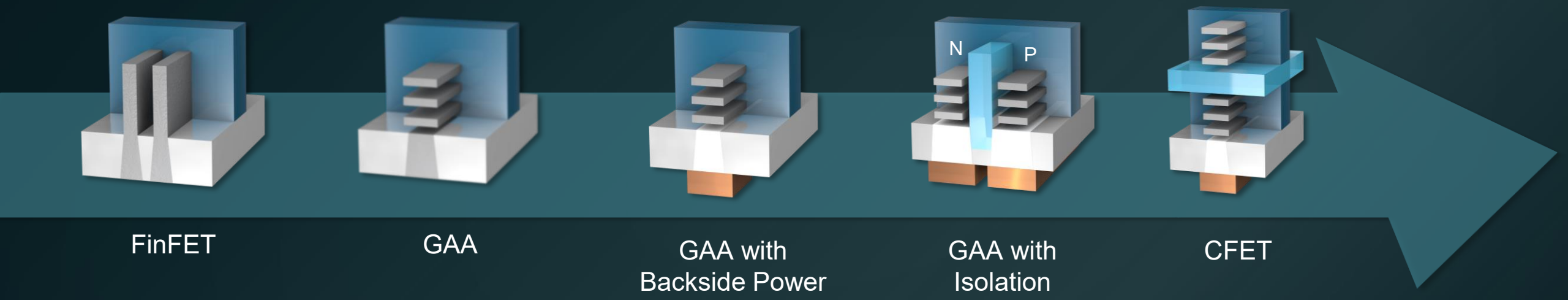
Logic Scaling Increasingly Supported with DTCO Innovations



Source: M. Liu/TSMC, ISSCC 2021

APPLIED MATERIALS

DTCO Driving Transistor Roadmap



FinFET

GAA

GAA with Backside Power

GAA with Isolation

CFET

FinFET : fin field effect transistor
GAA: gate-all-around
CFET: complimentary field effect transistor

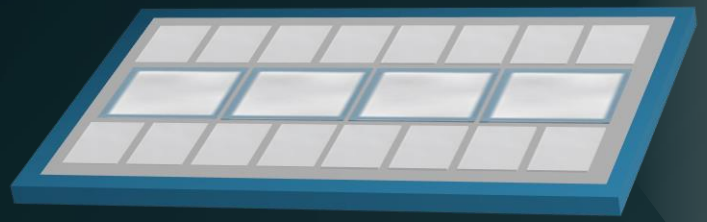
MASTER CLASS April 8, 2026

Logic Wiring

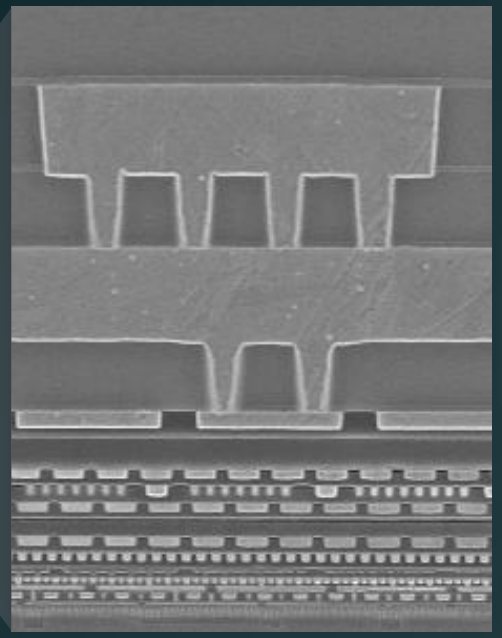
Zhebo Chen, Ph.D.
Senior Director
Metal Deposition Products
Semiconductor Products Group

APPLIED MATERIALS

Zooming in on Advanced Chip Wiring

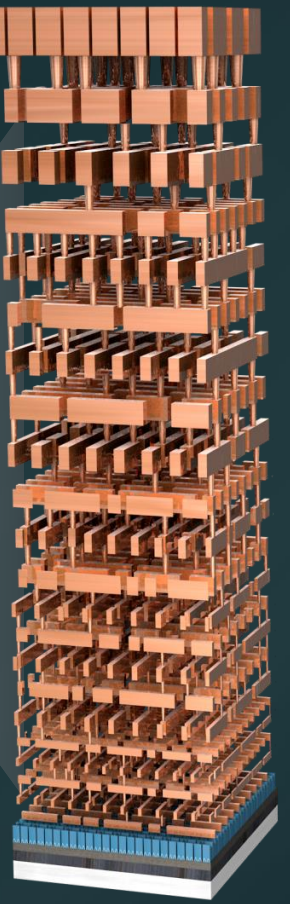


Advanced AI chip



Source: TechInsights

Microscope cross section view of chip



3D model of chip

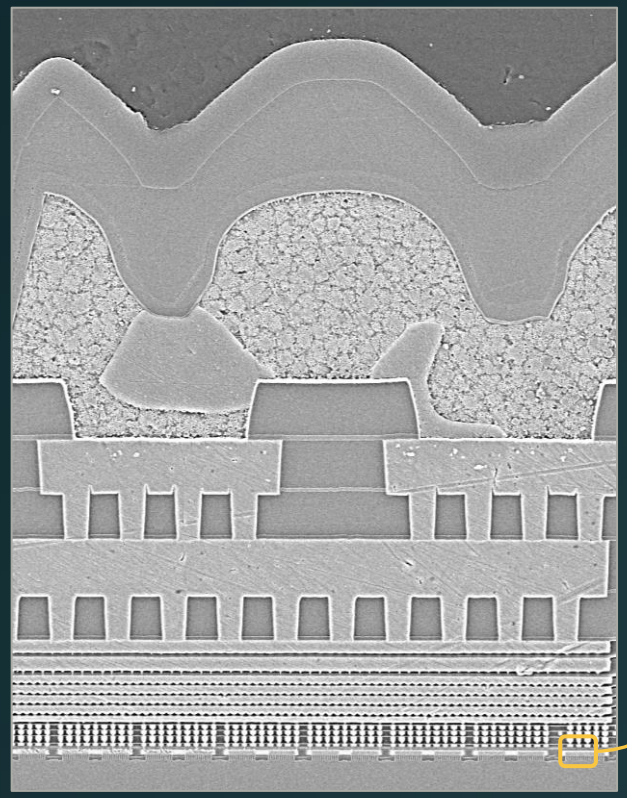
>20 layers
stacked copper interconnects

>2,000 miles
wiring

>300 billion
transistors

Source: TechInsights | Applied Materials estimates

Contacts Connect Transistors to Copper Interconnect Wiring



Source: TechInsights

Contacts

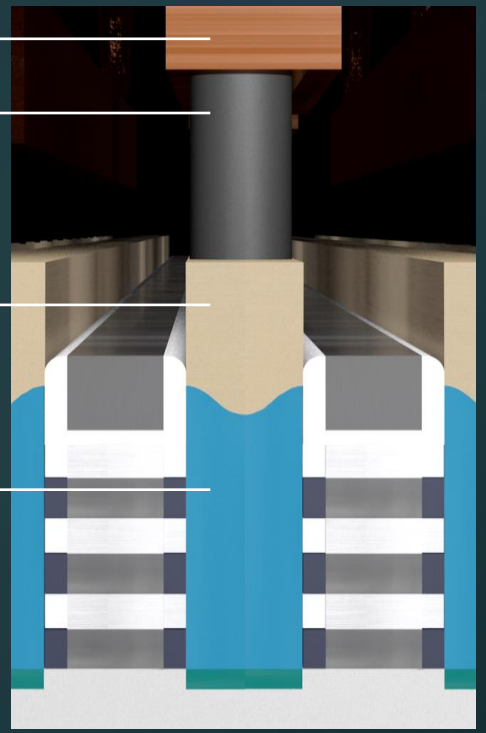
Source: TechInsights

Interconnect

Via contacts

Trench contacts

Transistor source/drain epitaxy



Contact Liner | Microwave Plasma Deposition

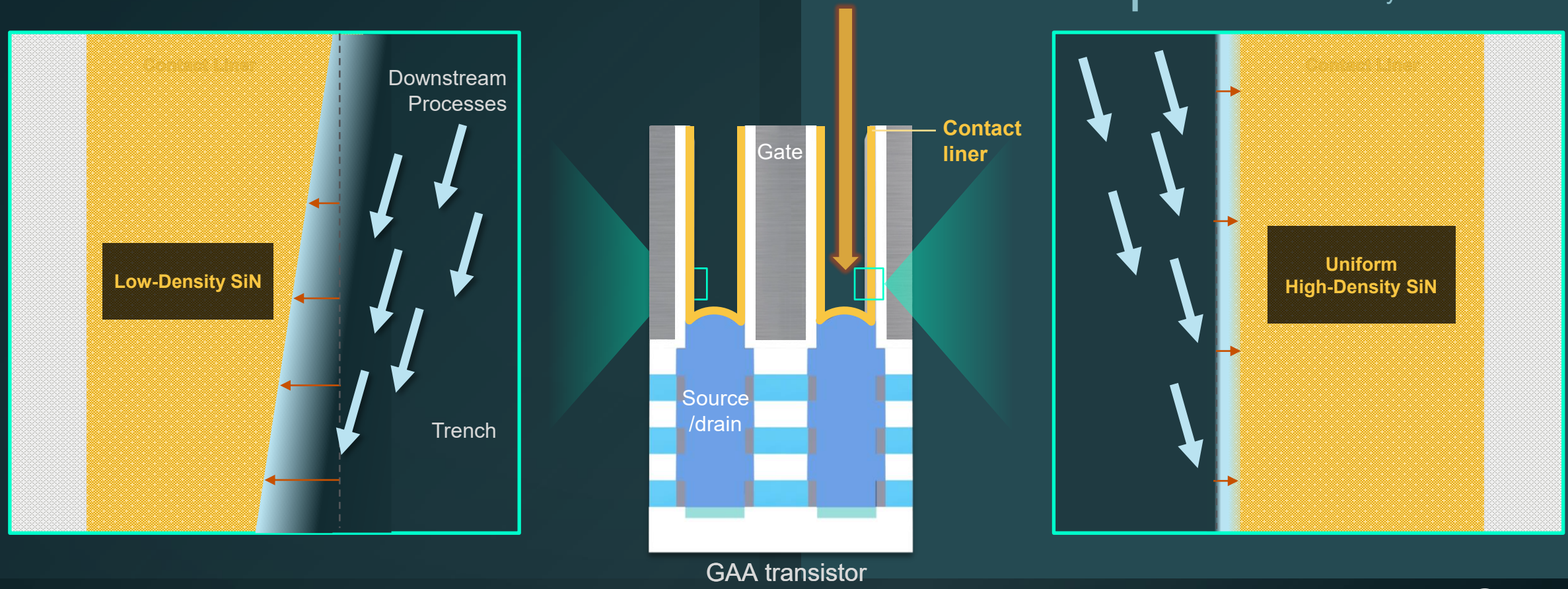
Conventional
Plasma Source

Downstream processes erode trench bottom when low-density contact liners used

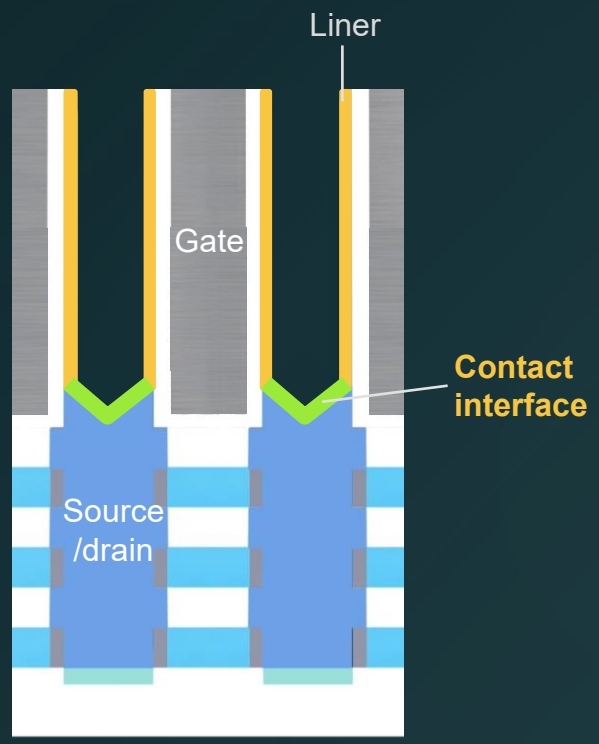
Microwave
Plasma Source

Downstream processes have minimal impact on trench bottom with new, high-density contact liner

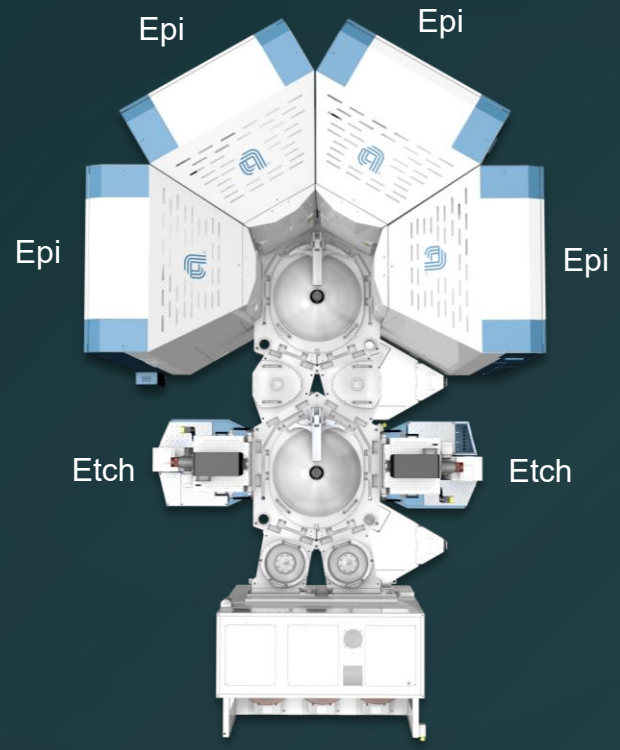
Advanced ALD SiN System



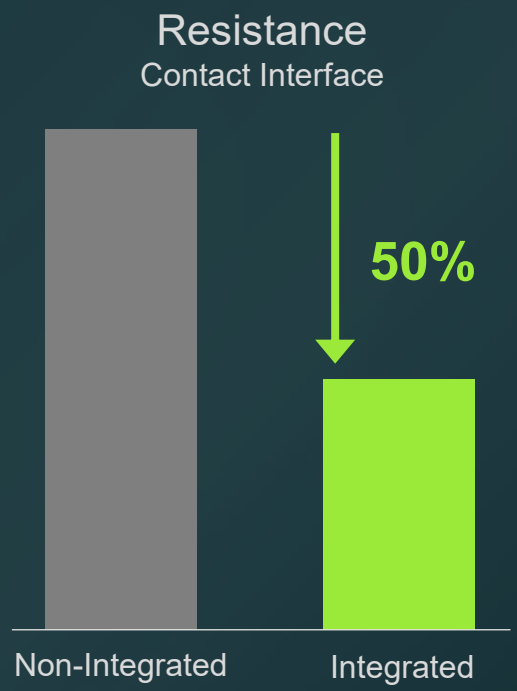
Contact Interface | Integrated Etch and Deposition



GAA transistor



New contact module platform
Integrated Materials Solution™

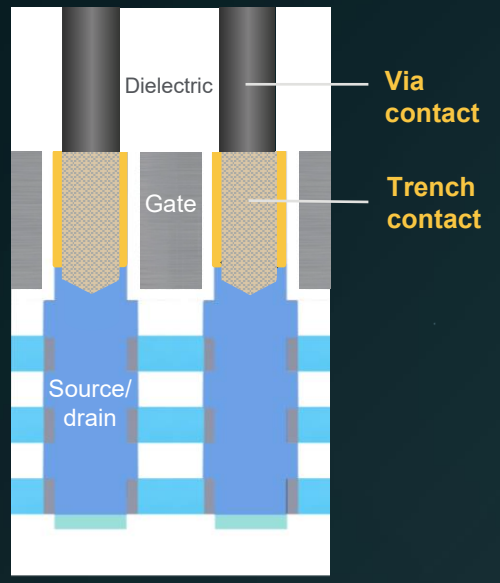


50% resistance reduction increases performance* by up to 5%

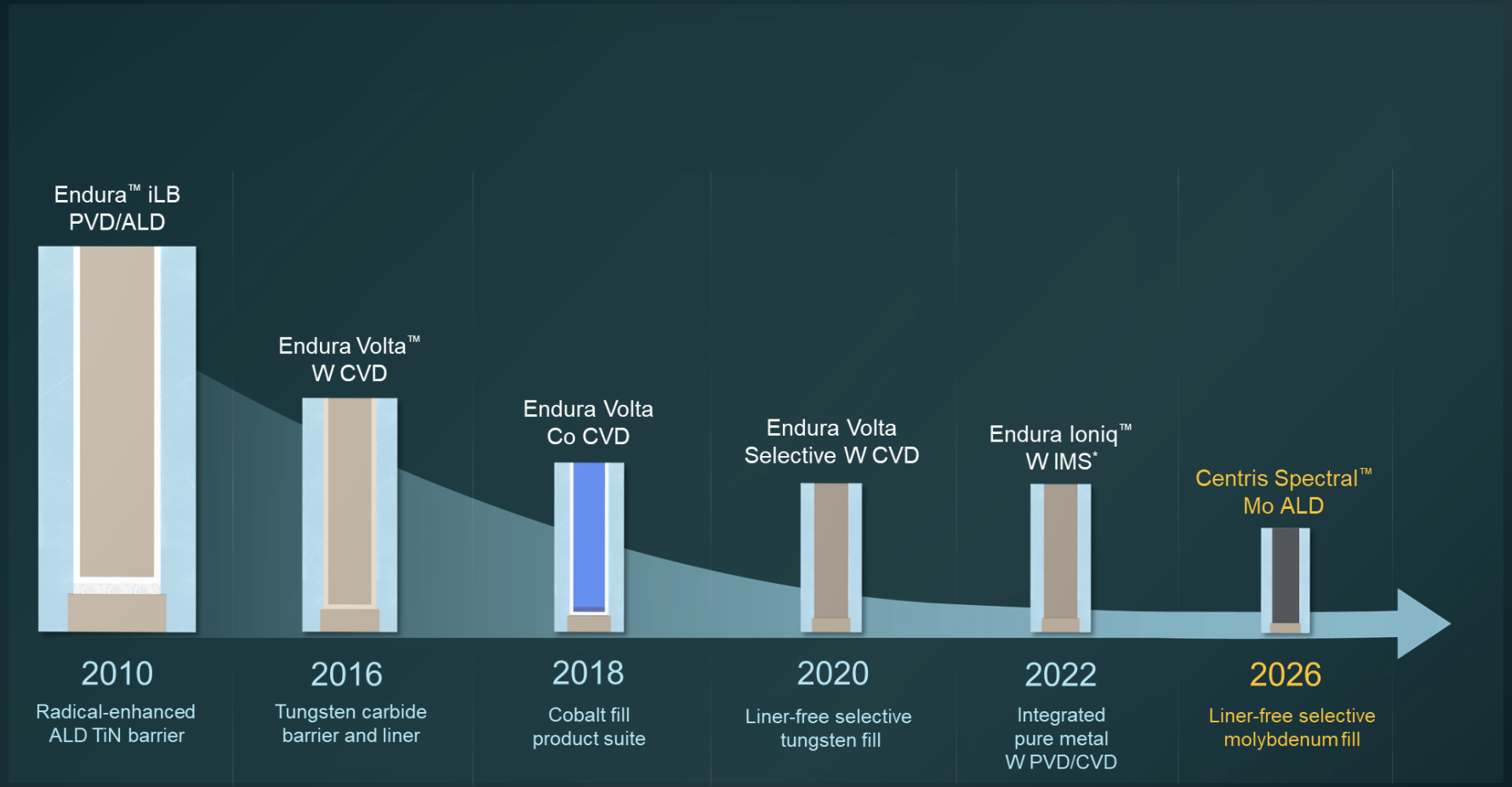
* PMOS Drain Contact Interface

APPLIED MATERIALS

Contact Metal | Contact Resistance Innovations

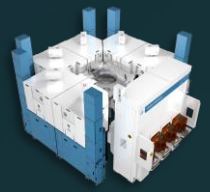


GAA transistor



APPLIED MATERIALS

Contact Metal | Process + Metrology + Digital Tools for Speed

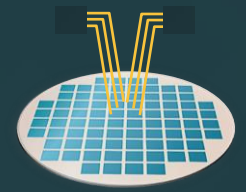


Spectral™ Mo ALD

Cross-Sectional
TEM~1-2 sites

Opta™ CMP

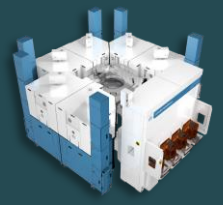
Cross-Sectional
TEM: ~1-2 sites



Electrical Testing:
>1,000 sites

(Weeks Later)

TRADITIONAL LEARNING CYCLE



Spectral™ Mo ALD

PROVision™ 10
>10,000 sites

AIX Digital
tools

Opta™ CMP

PROVision 10
>10,000 sites

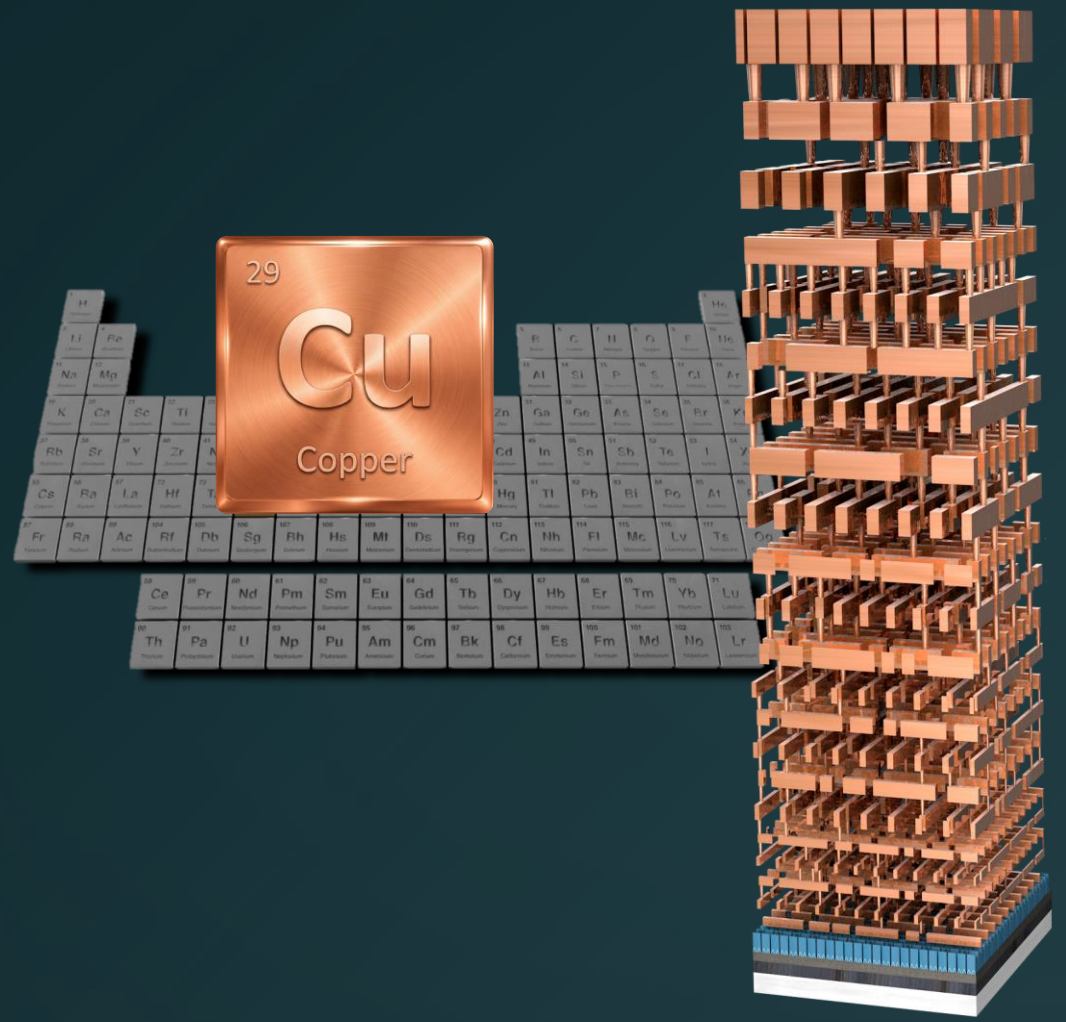
AIX Digital
tools

ACCELERATED LEARNING CYCLE

Close the Loop in
Hours versus Weeks

APPLIED MATERIALS

Interconnects Key to Chip Performance and Power



Interconnects | Routing of signals and power

Power consumption in AI chip:

Up to 50%

Opportunities:

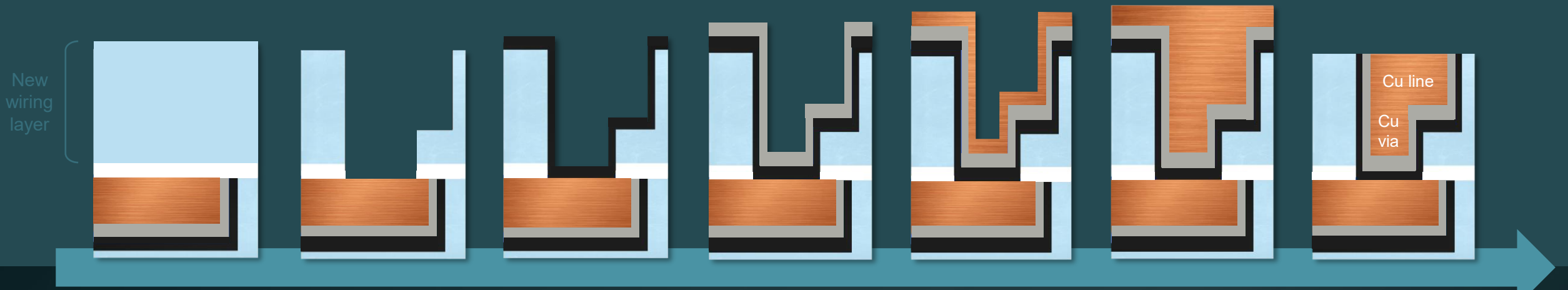
- Minimize power use
- Boost operating frequencies
- Remove timing bottlenecks

Contacts | Connecting transistors to interconnects

Transistors | High speed switching

Copper Interconnect Fabrication

Dual Damascene Process: Copper Wiring Requires Many Steps



CVD dielectric surrounds lines and vias for isolation

Dielectric etch forms wiring trench

PVD tantalum nitride barrier blocks Cu diffusion

PVD tantalum liner promotes Cu adhesion

PVD seed layer supports Cu growth

ECD copper fill

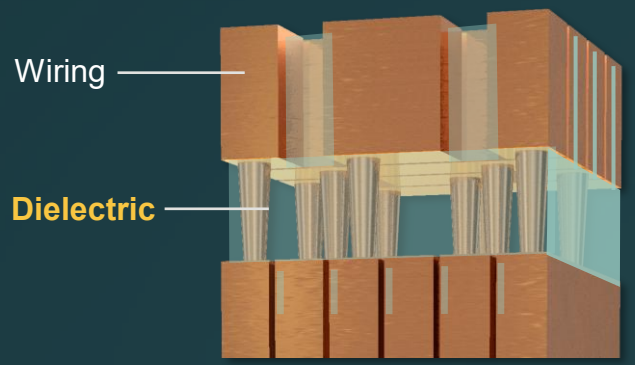
CMP removes Cu overfill

Endura™ CuBS: Copper Barrier Seed Integrated Materials Solution™

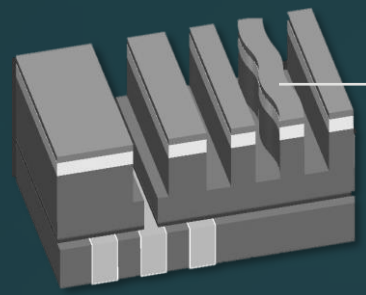
Reducing Wiring Capacitance | Low-k Dielectrics

Challenges

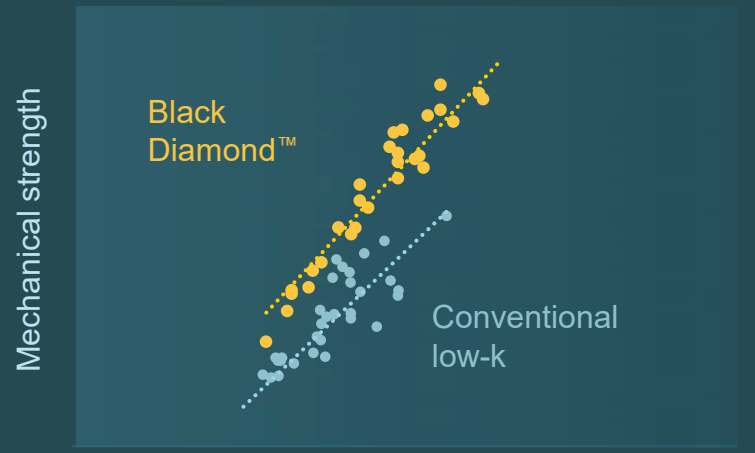
Reducing Capacitance with More Porous, Lower-k Dielectrics



Maintaining Mechanical Strength of Lower-k Dielectric Films



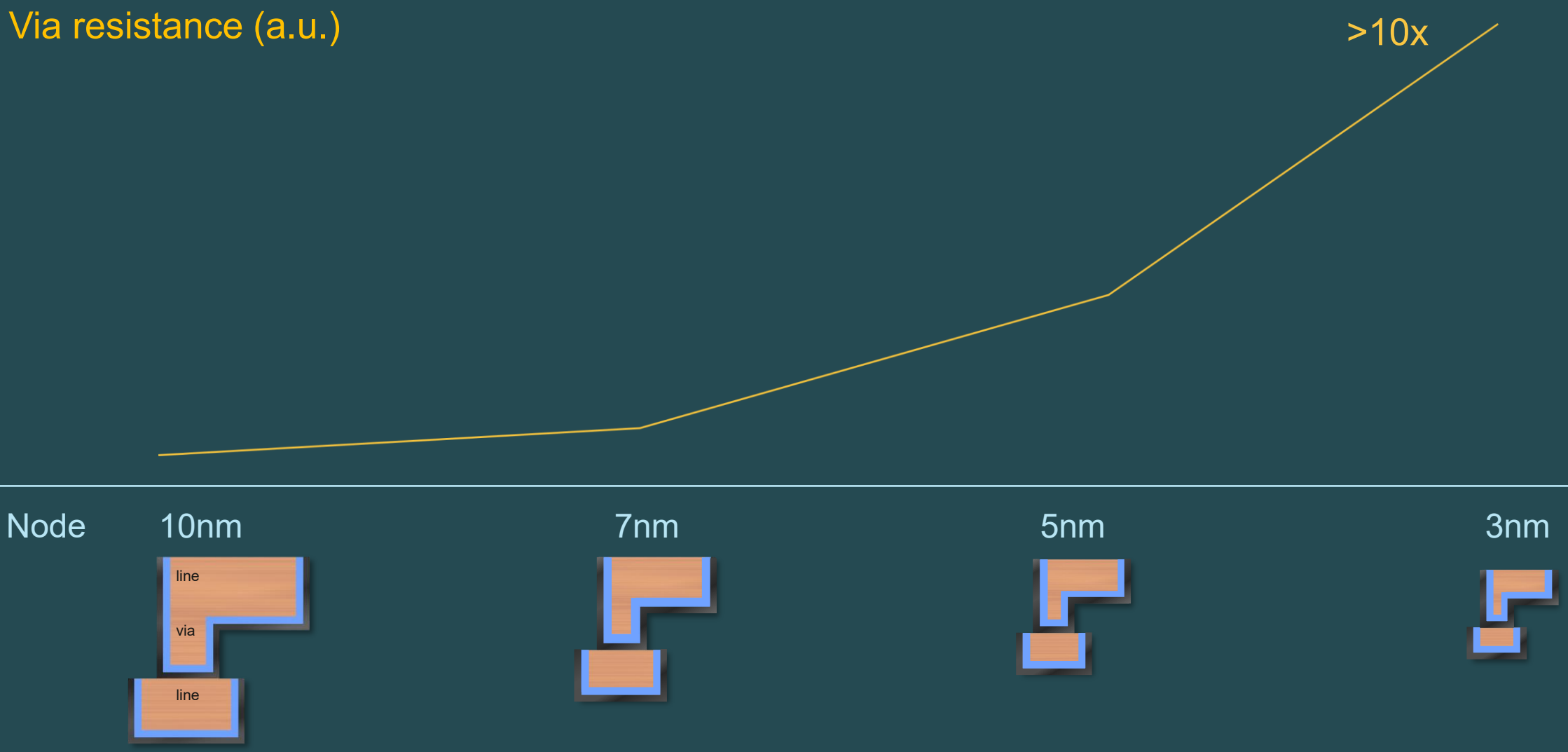
Increased risk of dielectric cracking during patterning and packaging



Producer™ Black Diamond™ PECVD

Source: Applied Materials

Scaling Wiring Increases Resistance

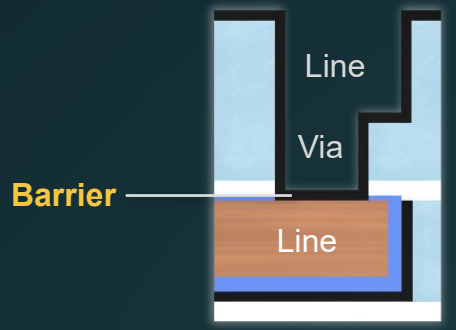


a.u.: arbitrary units

Reducing Resistance | Selective ALD Barrier

Challenge

Standard barrier integration

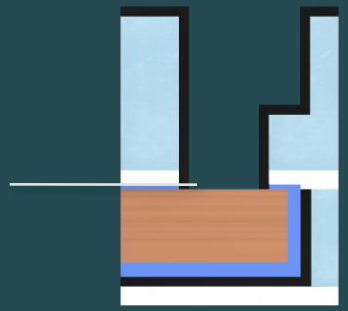


Via resistance increases up to 100%

from 5nm to 3nm node

Selective ALD barrier integration

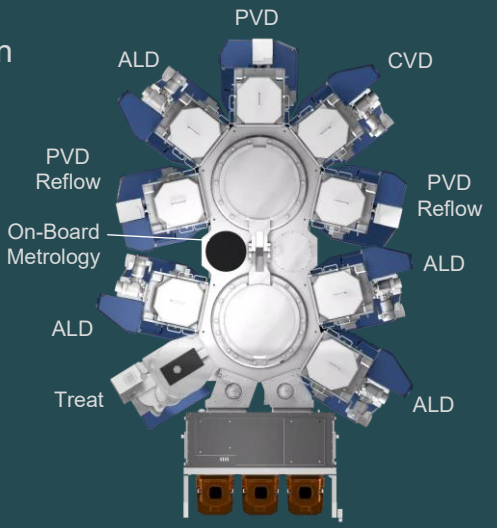
Eliminating barrier at bottom enables low-resistance copper-to-copper contact



Up to 50% lower via resistance

compared to standard barrier

- Copper Reflow
- Liner Deposition
- Materials Modification Treatment
- Integrated On-Board Metrology
- Selective ALD Deposition
- Interface Engineering
- Surface Preparation

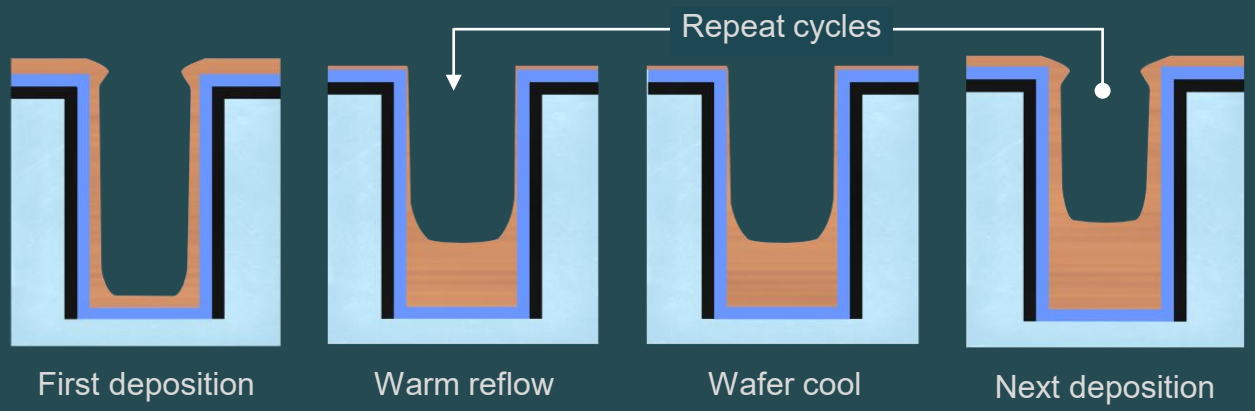


Endura™ CuBS™ IMS™

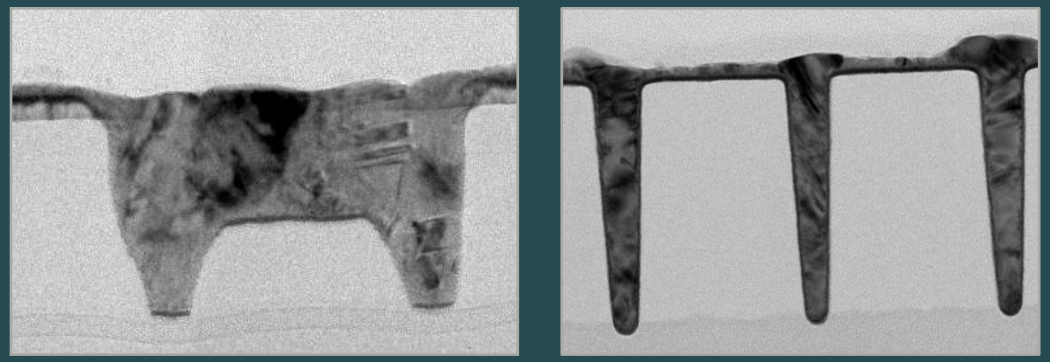
APPLIED MATERIALS

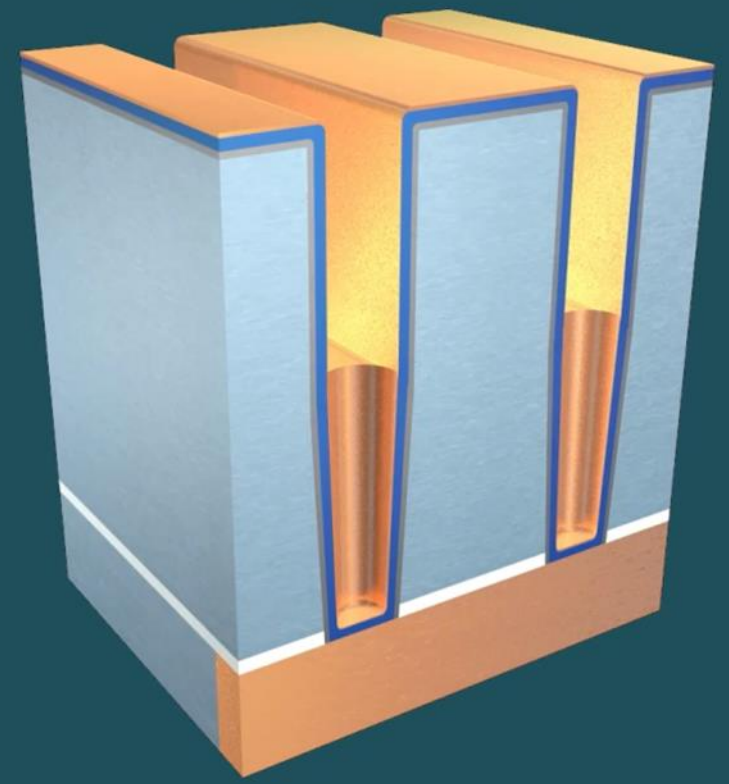
Reliable Copper Gap Fill | PVD Copper Reflow

Copper Reflow Sequence

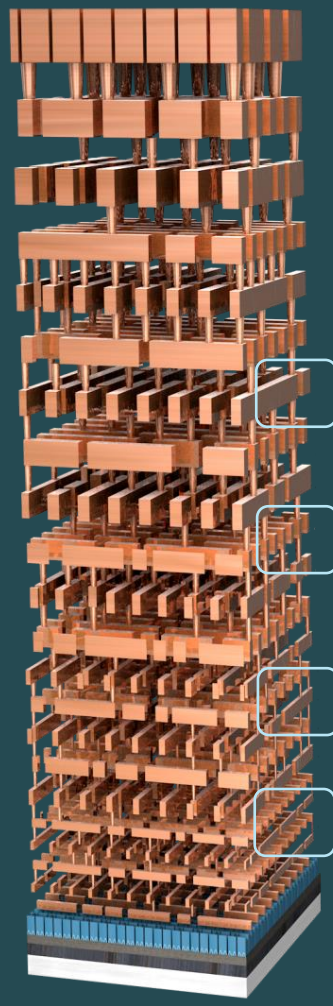


Complete Fill with PVD Copper Reflow

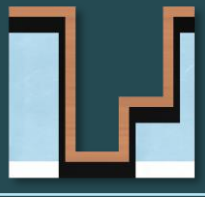




Innovations to Extend Copper Interconnects



Endura™ CuBS RF XT PVD
High-coverage barrier & seed



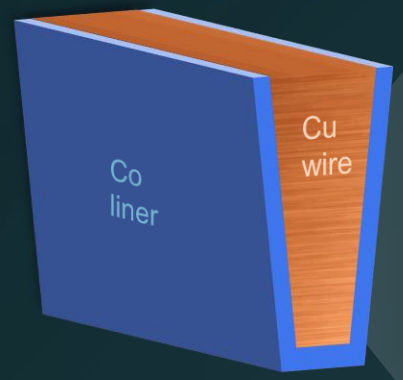
Endura™ Volta Cobalt CVD
Seed enhancing cobalt liner & selective metal cap

Endura™ CuBS ALD/PVD
ALD barrier

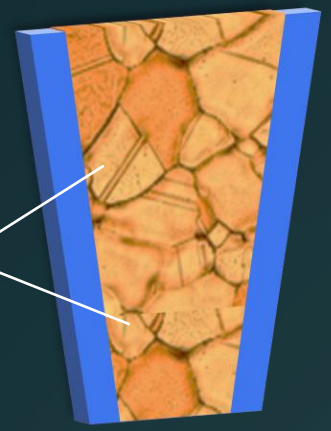
Endura™ Copper Barrier Seed IMS™
Selective barrier & binary liner

Reducing Copper Resistance | Radical and Anneal Treatment

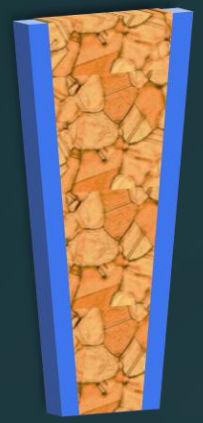
Challenge



Metal Layer

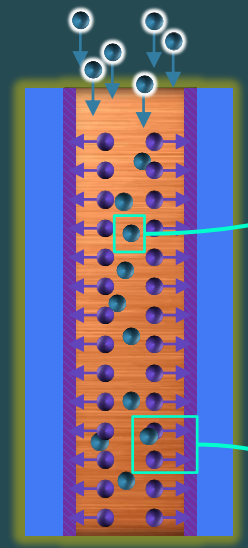


Wiring feature at ≥2nm nodes



Wiring feature at ≤2nm nodes

1. Radicals are introduced + heat is applied

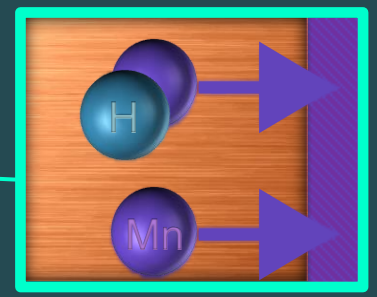


Hydrogen (H) radicals

Manganese (Mn)

2. Enhanced copper grain growth–reducing grain boundaries

Image source: Rogers Corporation



3. Mn dopants driven to surface where they enhance reliability

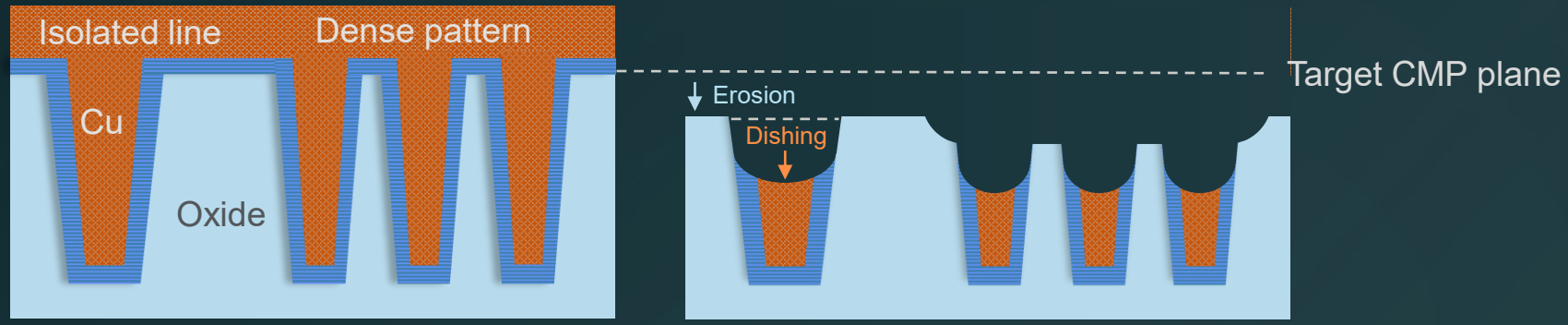
↓ >30% less resistance

Endura™ CuBS™ IMS™
Producer™ Viva™ Radical Treatment

APPLIED MATERIALS

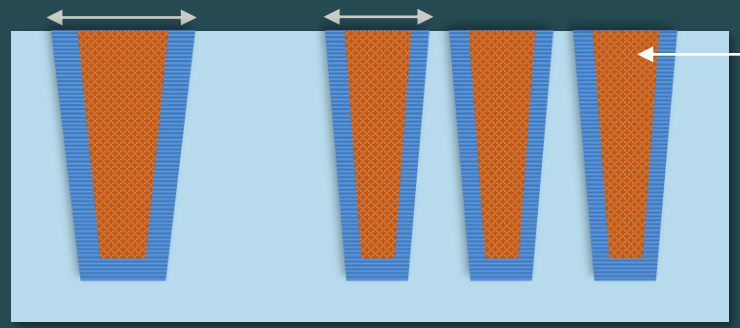
Reducing Copper Overfill | Chemical Mechanical Planarization

Challenge



Electrochemical Plating

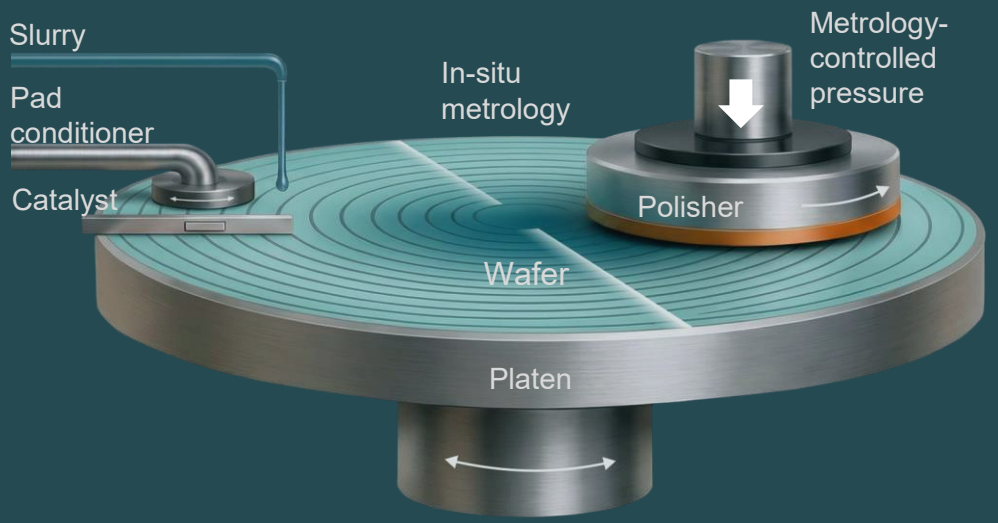
Defective CMP



No dishing or erosion

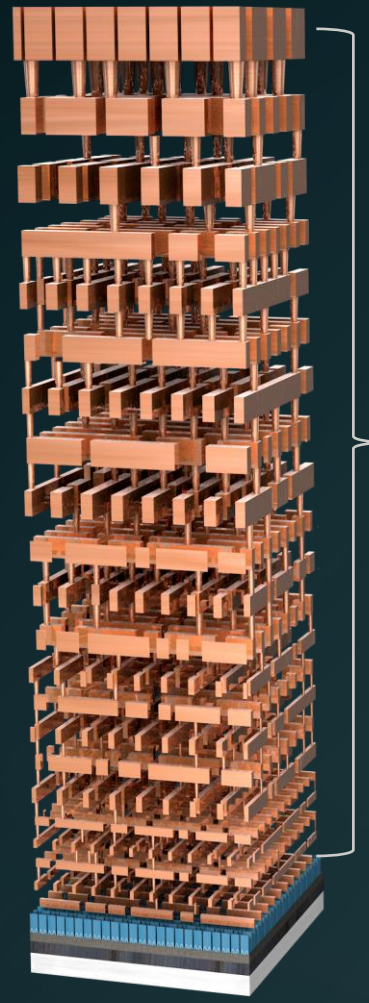
Metal Layer with Mixed Wiring Density

Opta™ CMP



APPLIED MATERIALS

Frontside Wiring Challenges in High-Performance Computing



Frontside Wiring
signal lines &
power lines

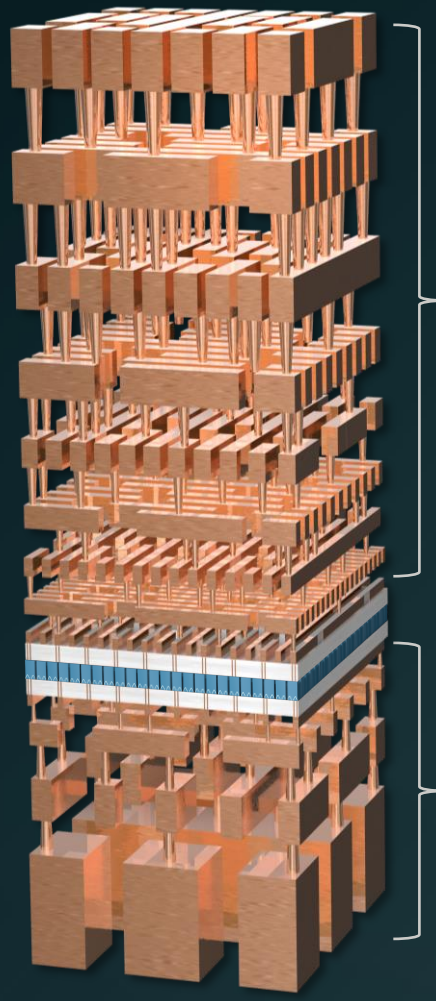
Conventional Frontside Wiring Stack

Wiring congestion

Power voltage drops by up to 50% as layer counts increase

Increased capacitance and reliability risks

Backside Power Benefits



With Backside Power Distribution Network

Reduced wiring congestion

Lower wiring resistance and power consumption

20-30% greater logic density at same lithographic pitch

MASTER CLASS April 8, 2026

Event Summary and EPIC Preview

Kevin Moraes, Ph.D.
Corporate Vice President
Strategy and Marketing
Semiconductor Products Group

APPLIED MATERIALS

KEY MESSAGES

AI is driving unprecedented demand for semiconductors and wafer fab equipment

Fastest growing areas of the WFE market are leading-edge foundry-logic, DRAM including HBM, and Advanced Packaging, where Applied has strong leadership

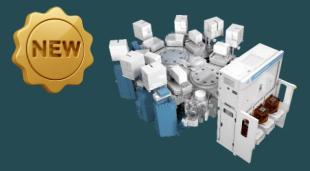
Materials engineering is increasingly key to roadmap inflections

Applied is ramping innovations that enable new transistors and wiring for energy-efficient AI

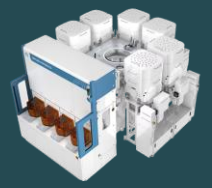
Inflection-focused innovation creates shared value for customers and Applied

Applied's Technologies at Forefront of Logic Inflections

NEW TECHNOLOGIES

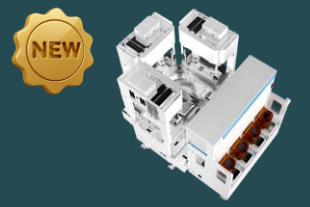


Trillium™
ALD



Sym3™ Z Magnum
Etch

Viva™
Radical Treatment



Precision™ Selective Nitride
PECVD

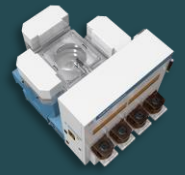
Spectral™ Moly
ALD

LEADERSHIP TECHNOLOGIES

Endura™ CuBS™
IMS™

PROVision™ 10
eBeam Metrology

Centura™ Xtera™
Epitaxy



Black Diamond™ Low-k
PECVD

Centura™ DPN HD
Treatment

Opta™
CMP

TECHNOLOGIES IN DEVELOPMENT

SiN Contact Liner
ALD

Contact-module Platform
IMS™

X-ray Analysis
Metrology

APPLIED MATERIALS

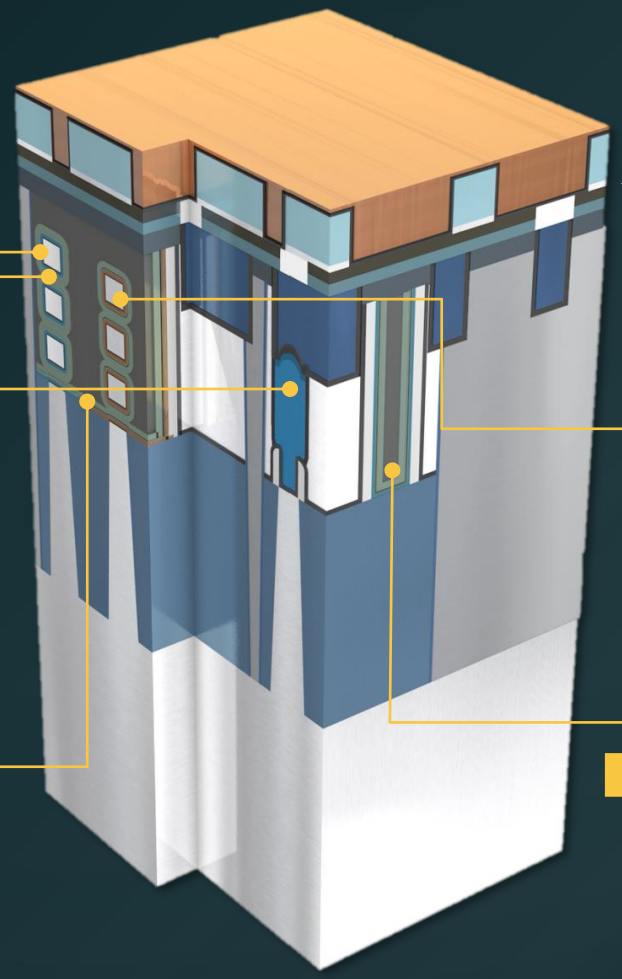
Key GAA Steps Enabled by Applied Materials

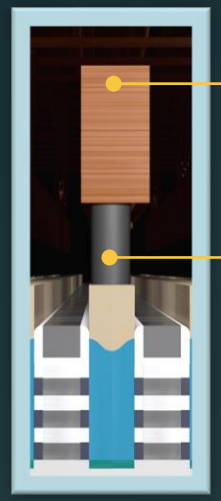
Creating Epi Nanosheets
Centura™ Prime™ Epi

Recessing SiGe
Producer™ Selectra™ Etch
PROVision™ 10 eBeam Metrology

Recessing Si and Depositing S/D Epi
Centris™ Sym3™ Z Magnum™ Etch
Producer™ Selectra™ Etch
Centura™ Xtera™ Selective Epitaxy

NEW
Protecting Isolation
Producer Precision™ Selective Nitride PECVD





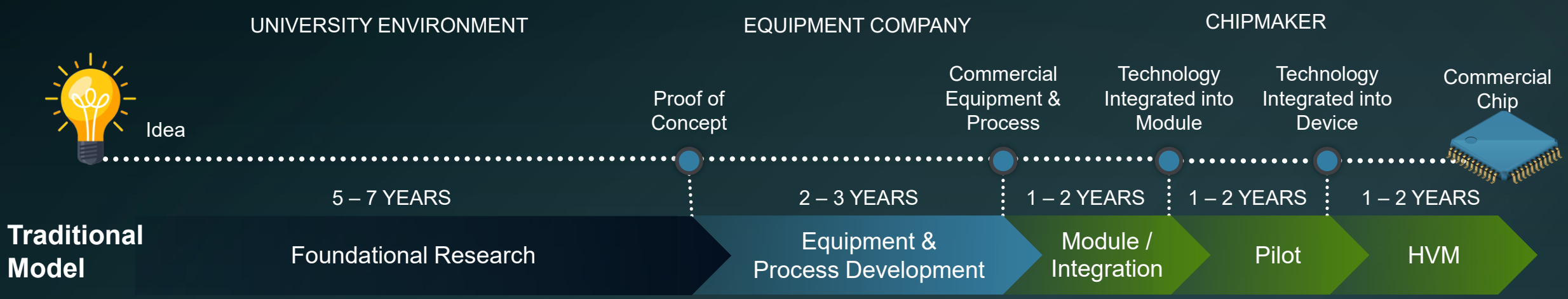
Planarizing Wires
Opta™ CMP

Creating Contacts
Centris™ Spectral™ Molybdenum ALD

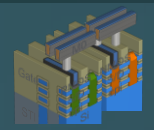
Removing SiGe
Producer™ Selectra™ Etch
PrimeVision™ eBeam Inspection
Producer™ Viva™ Radical Treatment
SEMVision™ Defect Analysis

NEW
Tuning the Gate
Endura™ Trillium™ ALD
Centura™ DPN HD

Complexity: Innovation to Commercialization Timeline

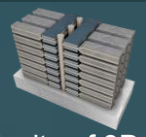


Can Take **10-15 YEARS** Today!



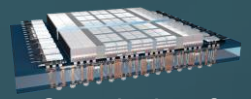
Complexity of GAA

- New **materials**
- New **processes**
- More **step-to-step interactions**



Complexity of 3D DRAM

- New **interactions**
- New **selective processes**



Complexity of Advanced Packaging

- New **technologies**
- More **interfaces**

EPIC Will Enable Faster Innovation and Commercialization

UNIVERSITY ENVIRONMENT

EQUIPMENT COMPANY

CHIPMAKER

Idea

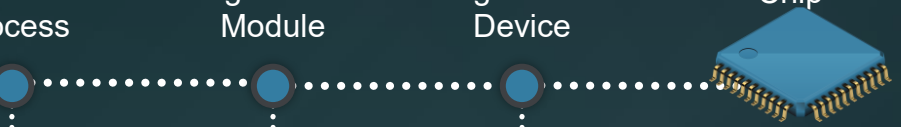
Proof of Concept

Commercial Equipment & Process

Technology Integrated into Module

Technology Integrated into Device

Commercial Chip



5 – 7 YEARS

2 – 3 YEARS

1 – 2 YEARS

1 – 2 YEARS

1 – 2 YEARS

Traditional Model

Foundational Research

Equipment & Process Development

Module / Integration

Pilot

HVM

New Model

EPIC

Foundational Research

Equipment and Process Development

Module / Integration

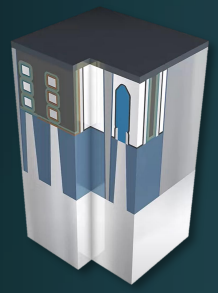
Pilot

HVM

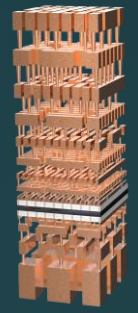
2x faster

All Semiconductor Inflections Going 3D

Leading-edge Logic

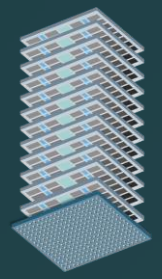


GAA Transistor



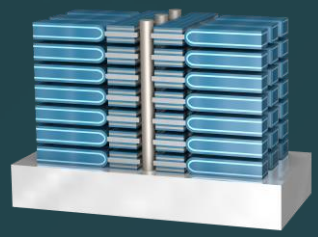
Backside Power

DRAM: HBM + Leading Edge



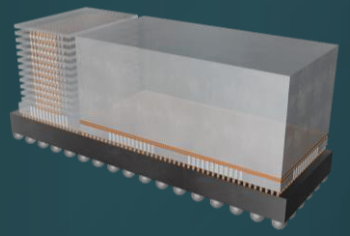
High-Bandwidth Memory

$4F^2$



3D DRAM

System Integration



Advanced Packaging

Applied's materials engineering technologies enable energy-efficient AI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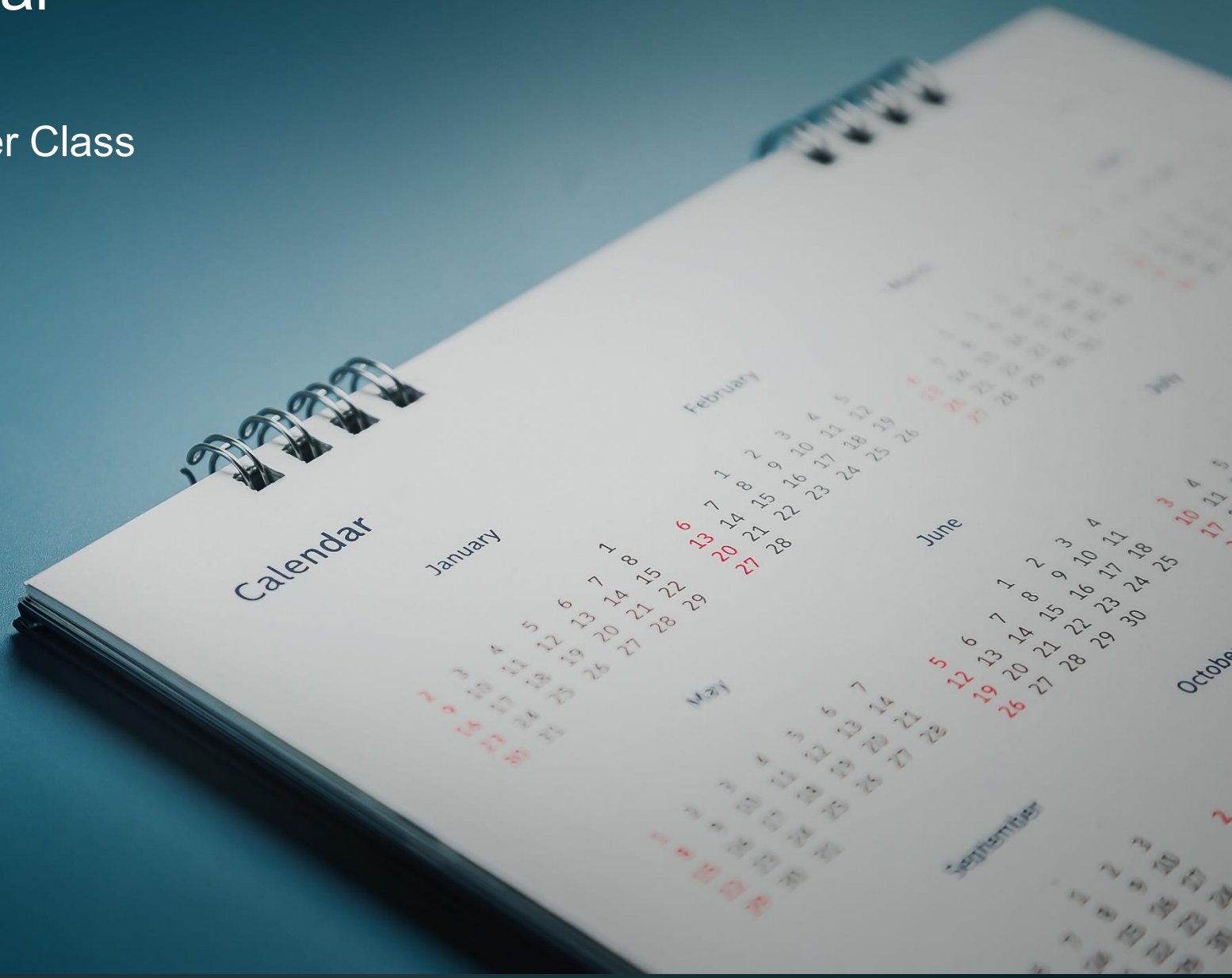
Inflection-Focused Calendar

JUNE 25 | 9AM PT
DRAM and Advanced Packaging Master Class
Webcast

OCTOBER 12
Investor Open House at the New
EPIC Center Silicon Valley
Sunnyvale, CA

OCTOBER 13
Investor Breakfast
San Francisco, CA | Webcast



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