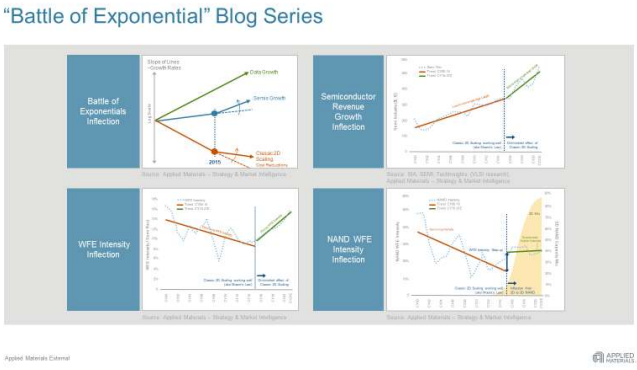
New Ways to Shrink Master Class

PREPARED REMARKS | April 21, 2022

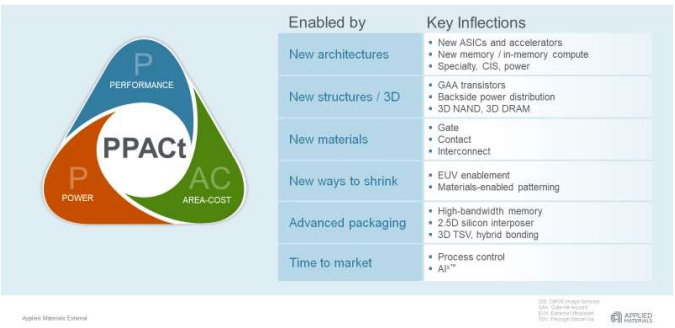
MICHAEL SULLIVAN | Corporate Vice President, Investor Relations

Hello and welcome to today's event. I'm Mike Sullivan, head of investor relations at Applied Materials. Over the next few minutes, I'm going to introduce our 2022 Master Class series.

The best place to start is with our demand thesis. As we've discussed in recent blogs, data is growing exponentially fueled by new applications beyond PCs and mobility. We're now in the fourth era of computing, fueled by the Internet of things, cloud computing and AI. At the same time, classic Moore's Law is slowing. This disconnect between the pace of data growth, and the pace of transistor scaling, is driving higher semiconductor and equipment spending -- across all semiconductor markets and nodes.



The industry's technology response to the slowing of Moore's Law is a "New Playbook" for driving continued improvements in chip performance, power consumption, area/cost, and time to market, which we call P-PAC-t. In our 2022 Master Class series, we'll elaborate on key elements of the New Playbook that will change the way chips are made in the years ahead. We'll forecast when these changes will happen, and how we expect them to affect equipment spending. We'll also relate these changes to Applied's growth opportunities – both in our 2024 financial model timeframe – and beyond.



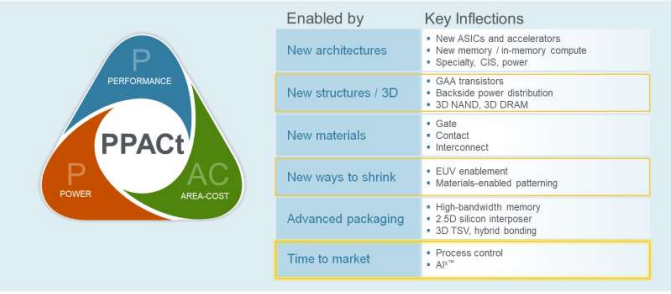
2024 Financial Model

	FY'20	FY'24 MODEL		
		LOW	BASE	HIGH
Revenue	$17.2B	$23.4B	$26.7B	$31.0B
Semi Systems	$11.4B	$16.2B	$18.4B	$21.7B
Services	$4.2B	$5.6B	$6.1B	$6.7B
Display	$1.6B	$1.6B	$2.2B	$2.7B
NON-GAAP ADJUSTED GM%	45.1%	47.5%	48.5%	48.8%
NON-GAAP ADJUSTED OP%	26.3%	30.6%	32.4%	32.7%
NON-GAAP ADJUSTED EPS	$4.17	$7.00	$8.50	$10.00

Today's class is called "New Ways to Shrink." We'll focus on the most obvious way to shrink, which is enabling EUV lithography. We'll also focus on a more subtle way to shrink, called DTCO. We'll show you how new 3D structures, like Gate All Around transistors and Backside Power Distribution, enable chipmakers to increase density in ways that go beyond lithographic scaling. And we'll show you how we can accelerate time to market of these new solutions using our eBeam metrology and AIx technology.

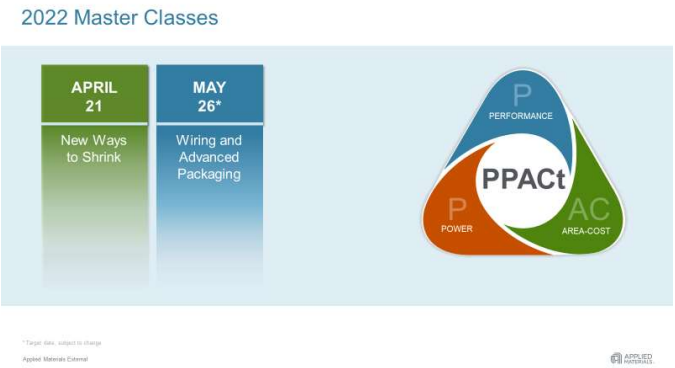
2022 Master Classes

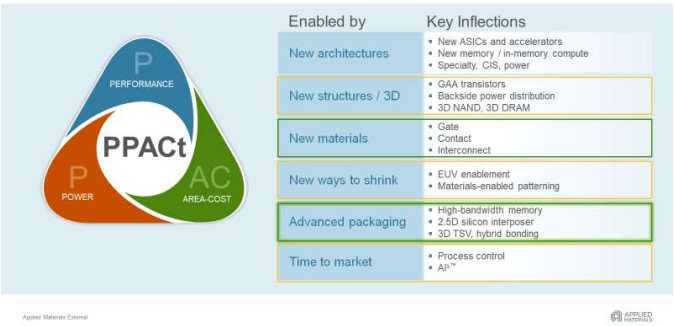
New Playbook for Power, Performance, Area-Cost and Time to Market



In May, we plan to hold our second Master Class, focusing on chip wiring, including the materials engineering breakthroughs our customers need as EUV reduces the space available for wiring. We'll go into the details of engineering backside power distribution. And we'll update you on advanced

packaging, which chipmakers and systems companies are using to help improve PPACt as Moore's Law slows.



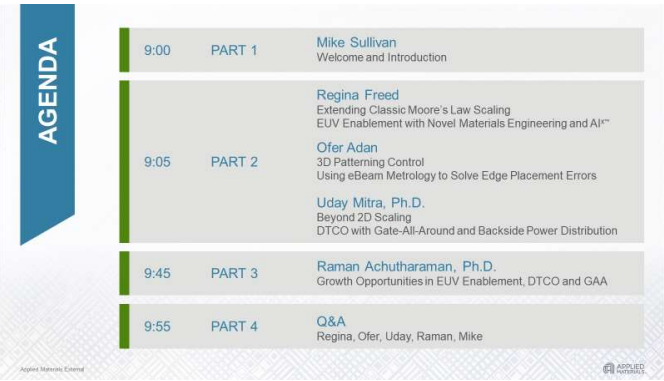


Finally, in the fall, we plan to hold our "Subscriptions and Services" master class. At our 2021 Investor Meeting, we set growth targets for our business under a range of WFE market levels. We hope the 2022 Master Classes will give you a better understanding of the inflections and solutions that drive our growth expectations in Semi Systems and AGS.

And here is today's agenda. In a moment, I'll pass the meeting over to Regina Freed who'll discuss new ways to continue classic 2D scaling by enabling and extending EUV. Next, Ofer Adan will discuss how

Applied is using eBeam technology to help customers continue 2D scaling and solve edge placement errors. Then, Dr. Uday Mitra will join us to talk about DTCO, including Gate All Around technology and Backside Power Distribution.

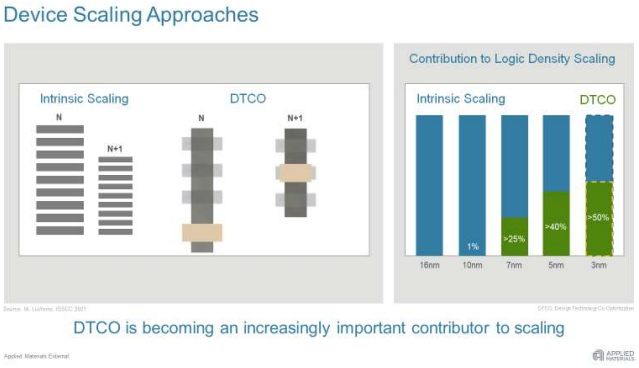
Finally, Dr. Raman Achutharaman will summarize how EUV enablement and DTCO will help Applied outperform our markets, through 2024 and beyond. After today's presentations, we all look forward to taking your questions. And with that introduction, Regina, it's over to you.



REGINA FREED | Vice President, Semiconductor Products Group

Thanks Mike.

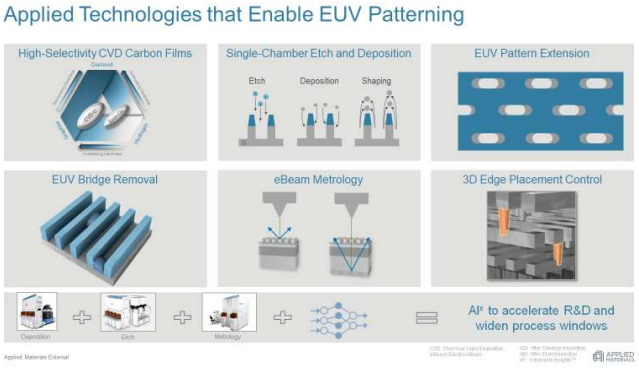
In today's Master Class, we're going to cover two ways to shrink. The two ways are summarized in a paper that one of our customers presented at last year's ISSCC conference. On the left, "intrinsic scaling" refers to classic 2D Moore's Law. I'll focus on that part of the discussion. In the middle, DTCO stands for design technology cooptimization. This is the clever rearrangement of logic elements to enable further scaling -- independent of lithography pitch. Uday will focus on this part of today's Master Class. On the right, our customer states that in the future, about half of density improvements will come from intrinsic scaling, and half will come from DTCO.



Over the years, lithography advances and materials engineering techniques evolved together to help us shrink features and increase density. Deep UV immersion lithography enabled 80nm features. When the lithography roadmap stalled, the industry developed self-aligned double patterning, and quadruple patterning, to enable 40nm features and then 20nm features. EUV was a big step forward, giving us the ability to create 25nm features with a single litho pass. Today, we need even smaller features, and EUV double patterning is already being used. For the future, high NA EUV is on the roadmap to replace EUV double-patterning with a single litho pass.

On the materials engineering side, a number of changes need to be made to enable EUV scaling to continue. We call this EUV enablement, and we'll discuss 7 of these innovations today. One, we need to change the material used to transfer EUV patterns to the wafer. This is a change from spin-on hardmasks to CVD hardmasks.

Two, we need a new kind of etch technology that can deposit and remove material inside the same chamber to improve the quality of the lines made with EUV. Three, a new directional patterning technology can be used to extend EUV patterns to help increase EUV yields and reduce EUV costs. Four, we can also use our directional patterning technology to remove the bridge defects that occur as the lines made with EUV get closer together. Five, as my colleague Ofer will explain today, we need to use eBeam metrology in the after-development and after-etch stages of EUV patterning to increase EUV pattern uniformity across the wafer. Six, we also need 3D eBeam metrology to control edge placement among layers, which gets incredibly challenging as the critical layers shrink with EUV. Finally, I will explain how we use Applied's AIx technology to speed EUV process development and widen process windows to increase yields.



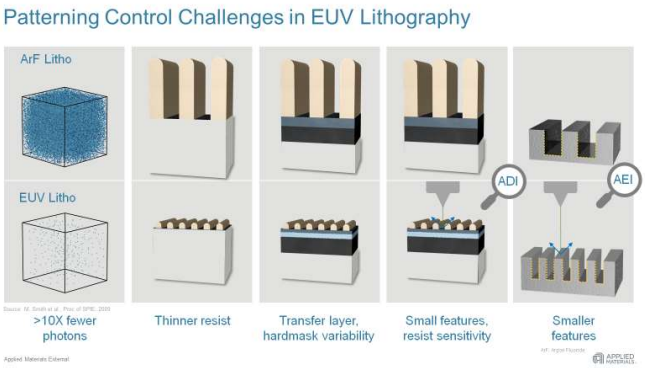
Next, I'll give you a quick summary of the patterns we are making and shrinking with EUV. Modern patterning of the finest layers of a chip begins with uniform lines and spaces that run in a single direction. A second mask, called a cut mask, determines where the lines are segmented to help define individual features, such as the fins in a FinFET transistor. A third mask defines the location of the vias which are holes that can be filled with metal to connect one layer of the chip to the next. Precisely replicating and placing these lines, spaces and vias on each layer of the chip is critical to wafer yield and chip performance and power. With each shrink, the challenges increase.

Now let's get specific about how we transfer mask patterns to the wafer. The litho scanner sends photons to the photomask. Photons are bounced off the mask and onto the photoresist which absorbs the mask pattern, much like a photograph. The photoresist is developed which creates openings in specific locations so that the desired pattern can be transferred to the next layer. The photoresist is measured to make sure the pattern is correct before it is etched into the wafer. This is called after-development inspection or ADI. We look to make sure the critical dimensions of the pattern are uniform. We also check the overlay, making sure the pattern is correctly centered over the wafer. If the ADI looks good, we commit to etching the wafer.

In fact, photoresists are far too delicate to withstand the etching that transfers the pattern to the wafer. So between the photoresist and the wafer, we deposit a transfer layer and a hardmask. The transfer layer is optimized to receive the pattern from the photoresist layer quickly and precisely before the etching fully erodes the photoresist. The hardmask receives the pattern from the transfer layer and is even more resilient. It's engineered to withstand the etching until the pattern is fully replicated in the

wafer. Then, the wafer is measured in a step called after-etch inspection or AEI. If all of the materials engineering is successful, then the ADI measurements from the photoresist and the AEI measurements from the wafer will be highly consistent. You'll notice that with EUV lithography, the photoresist layer is much thinner. There are two reasons for this.

First, EUV has more than 10 times fewer photons then DUV, so we need a thinner resist that can fully absorb the mask pattern using far fewer photons. Second, the EUV lines are very narrow. If the photoresist was thicker, then these line patterns could collapse. Now let's talk about the first inflection we're covering today: The transition from spin-on pattering films to CVD films.



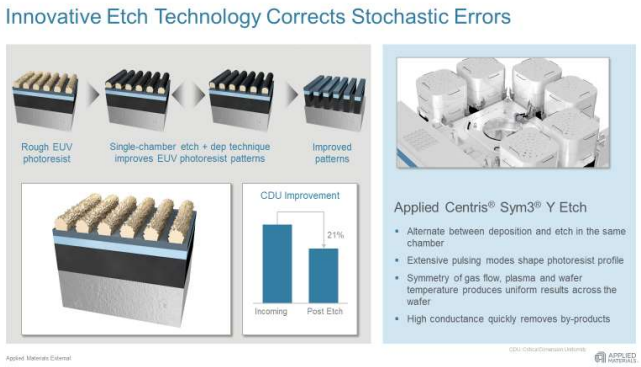
Traditionally, the underlayer and hardmask are deposited using spin-on deposition technology, which is fast and cost-effective. However, to enable further EUV scaling, we need to replace the spin-on films with new films deposited using chemical vapor deposition, or CVD. The emerging problem with spin-on deposition films is that they begin as a liquid and are inherently soft. Soft films are less resilient to etching. Also, with spin-on techniques, it becomes difficult to control the film's thickness with perfect uniformity across the entire wafer. CVD deposition has more available process variables that can be tuned to control the hardness and uniformity of the films across the 300mm wafer.

Today, we are introducing Stensar CVD advanced patterning film for EUV that is deposited with our Precision system. Our Stensar films can be engineered for specific levels of resilience. Stensar films can also be tuned for selectivity to specific etch chemistries. This helps further tune etching speed and EUV pattern fidelity. Our Stensar films are used for both the underlayer and the hardmask. Today, we are seeing strong customer adoption of Stensar over spin-on films.

Now let's talk about today's second EUV enablement inflection, which is about etch innovations. The lower number of photons in EUV creates what we call stochastic errors, which create variability in the photoresist and in the lines, spaces and vias being patterned. The smaller the EUV patterns, the larger the stochastic errors as a proportion of the features we are trying to make. If these irregularities are transferred to the wafer, we can have gaps in lines -- which cause open circuits -- bridges between adjacent lines, which cause shorts -- and edge placement errors between the various layers of the chip -- which reduce yield. Importantly, we can use materials engineering to correct stochastic errors and help enable EUV scaling to continue.

I'll give you a great example. We have developed a special technology in our Sym3 etch systems that allows us to alternate between etching and depositing material within a single chamber. We use this to gently remove and deposit materials in the same chamber as we transfer the EUV pattern to the hardmask. This unique approach averages out pattern variations and creates smoother features. Using it, we can actually heal stochastic errors before we etch the wafer.

Now I'll show you an animation of how this unique process works. Personally I think EUV is amazing, and I think this ability to make EUV even better with materials engineering is equally amazing.



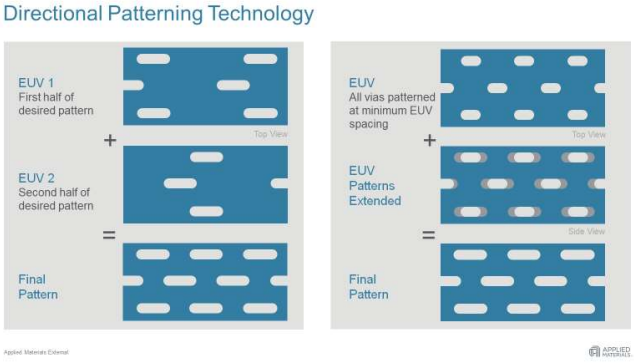
Applied's Sym3 etch technology was originally targeted at memory applications, but today, we have very strong adoption in logic, particularly at the most advanced EUV nodes. The reason is reflected in the name. Sym 3 provides symmetry in gas flow, plasma and wafer temperature, and this helps us to tightly control the etch and deposition processes and achieve very even results across the wafer. The

Sym3 chambers also have high conductance, meaning we can quickly remove all of the etch by-products from the chamber, which gives our customers higher yields.

Raman will show you how quickly we are growing in the patterning etch market.

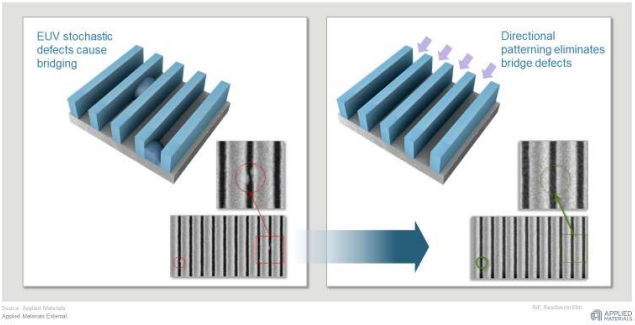
Now let's talk about today's third inflection. We've developed an exciting technology that can help create patterns that are tighter than the resolution limits of EUV. What this means is: we can give customers patterns that would otherwise require EUV multipatterning. Our technology is called directional patterning, and I'll give you one example of how it can be used. One of the most critical patterns is vias which connect the metal wiring of one layer of the chip to the next.
Landing these vias atop one another with good edge placement is key to yield and also helps improve performance and power. Customers prefer elliptical vias because they are easier to land than smaller, rounder vias. To continue scaling with EUV, we need to get the tips of the vias as close together as possible. First, I'll describe how to create a desired pattern using EUV double patterning. We divide the pattern in half so that the via tips in each pattern are within the resolution of EUV.

Then, we use two EUV exposures to transfer the entire pattern to the wafer. Using Applied's new approach, we create one mask that has all of the vias, observing the tip-to-tip distances needed by EUV. Then, we use our lateral patterning technology to precisely extend the tips in both directions until the tip-to-tip placement is ideal. We have more ideas of how we can use lateral patterning to extend 2D scaling below the limits of EUV. Customers are now evaluating our technology to extend 2D scaling while increasing yields and reducing EUV costs.



Next I'll quickly cover a fourth inflection. As EUV lines and spaces get narrower, we have more potential for bridge defects that cause shorts. Another promising use of our lateral patterning technology is to remove unwanted material from the hardmask to heal the patterns before they are etched into the wafer, thereby increasing EUV yields. This capability is now being used to accelerate R&D, and it has potential for volume production. Applied's directional patterning technology is unique in the industry, and we'll share more details over time as we refine these new applications with our customers.

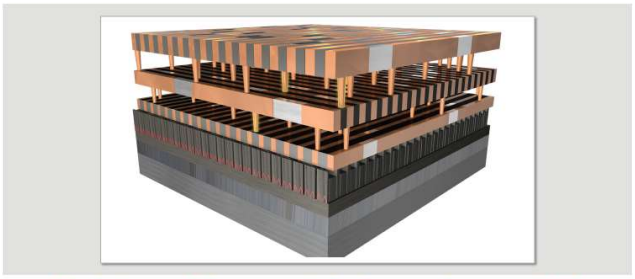
Directional Patterning: Stochastic Defect Removal



As you have seen from these examples, there is a strong interdependence between lithography and materials engineering. The patterns on the EUV masks are not the patterns on the wafer unless we tune all of the materials deposition, modification and removal steps to ensure pattern fidelity on the wafer. The uniformity needs to be good locally -- meaning within the chip -- and across the wafer, so that most of the chips yield regardless of their location. In the past, the industry focused primarily on 2D pattern fidelity with techniques like holistic lithography that work on optical corrections, one layer at a time.

As we continue to shrink features using EUV, increase the process steps on each layer, and use more 3D design techniques, we need to supplement 2D optical techniques with 3D methods. Ofer will explain some of the new ways we are enabling further EUV scaling by supplementing 2D optical methods with eBeam.

Edge Placement: A Growing Challenge



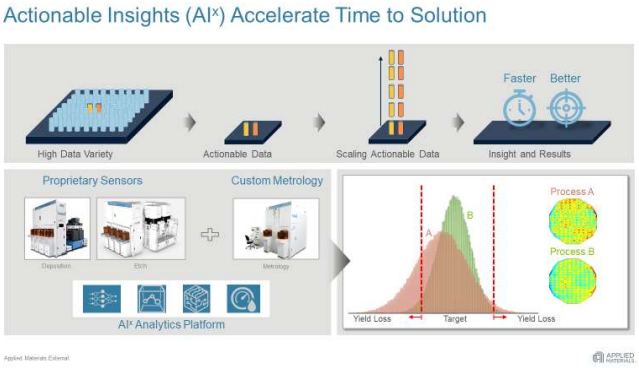
3D metrology needed to overcome stochastic errors and process variability

I'll close my section by explaining how we are applying the breadth of Applied's portfolio along with cutting edge data science to extend 2D scaling into the future. With Applied's AIx technology platform, we are deploying hundreds of sensors in our chambers and systems to measure all of the process variables that can affect pattern fidelity and uniformity. We've put metrology into our deposition systems so we can measure the quality and thickness of films as they are being created, in vacuum.

And we use PROVision e-Beam metrology to measure the on-wafer results of all of these processes. Then we use AI analytics to tease out the optimum combination of process variables that produces the ideal on-wafer results using the widest possible process window. It's not just one layer at a time: it's

holistic analysis of the interdependencies across all of the critical layers. Solving this multi-dimensional optimization challenge is the key to faster time to market and higher yields in production. AIx is designed to accelerate process R&D by 2X and widen process windows by 30 percent. It is a very powerful new way to enable further EUV scaling by controlling materials engineering and edge placement.

Thank you for listening, and now I'd like to hand the meeting to Ofer to discuss the E-Beam inflection.

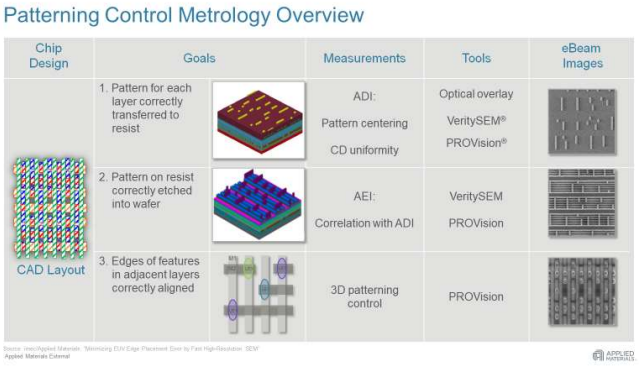


OFER ADAN | Senior Director, Process Diagnostics and Control Group

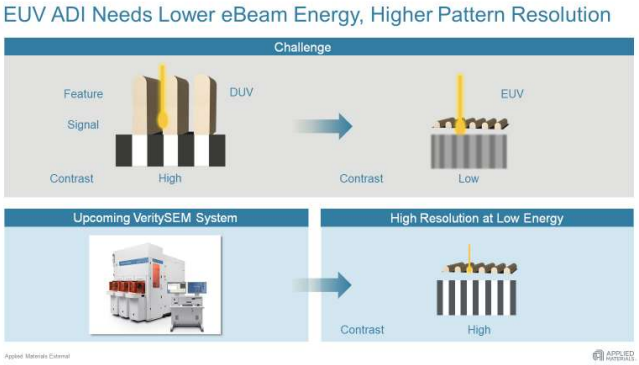
Thank you Regina.

To continue the 2D scaling roadmap, we need to ensure three things. One, we need to make sure the intended patterns on the EUV photomask are precisely replicated on the photoresist, with proper features, centering and uniformity across the entire wafer. We perform after-development inspection -- or ADI -- to find serious errors before etching the wafer. Second, we need to make sure the patterns we etch into the wafer are just as uniform. We use after etch inspection -- or AEI -- looking for very high correlation between the ADI and AEI measurements. Any inconsistencies introduce irregularities that can propagate as we continue to process the wafer.

Third, we need to align the edges of the critical features on each layer of the chip with their opposite features on the layers above and below. Edge placement errors can ruin entire wafers, or they can crop up in particular areas and negatively impact chip yield, power and performance. I'll show you how we are deploying eBeam technologies in each of these three areas. And later, Raman will show you how the eBeam inflection is driving growth for Applied Materials.



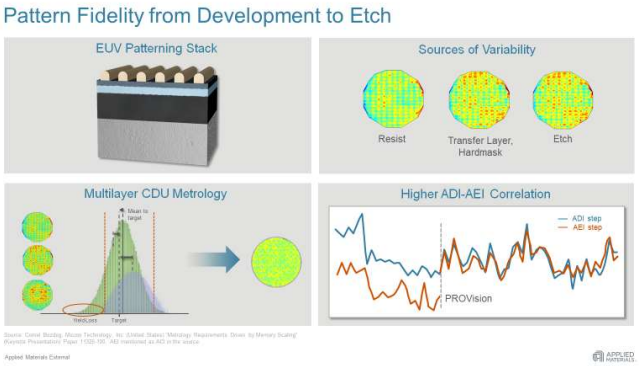
Let's begin with after-development inspection or ADI. As Regina showed us, the EUV photoresist is much thinner than DUV resists. If we used conventional eBeam systems and energies to look for stochastic defects and measure the critical dimensions and overlay, we could distort the patterns on the delicate resist. To help customers inspect more during ADI, we're preparing to introduce a new version of our VeritySEM system that has unique capabilities for emerging EUV nodes. We use lower energy to minimize interaction with the resist. And we provide a unique technology that improves EUV pattern image resolution, giving us sharp dark and light contrasts at low energy. Customers are already using this technology to ensure CD uniformity at emerging EUV nodes, and to center the mean of pattern variation across the wafer prior to etching.



Next, let's discuss pattern fidelity, from development to etch. In easier times, if engineers properly centered the photoresist pattern over the wafer, they could usually count on good etch results as well. But as Regina explained earlier, EUV patterning introduces a number of intermediate steps. The photoresist pattern is etched into a transfer layer, then the transfer layer pattern is etched into a hardmask, and finally the hardmask pattern is etched into the wafer. Each of these intermediate steps is a potential source of variation that can reduce pattern fidelity on the wafer. And this can cause serious ADI to AEI correlation issues.

To help with EUV scaling, engineers are now adding metrology steps using our PROVision eBeam metrology system which is 10 times faster than SEM metrology. PROVision can generate data for each of these intermediate steps, giving process engineers bias signature data that they can use to holistically center the entire patterning flow. Engineers can quickly improve ADI-to-AEI correlation,

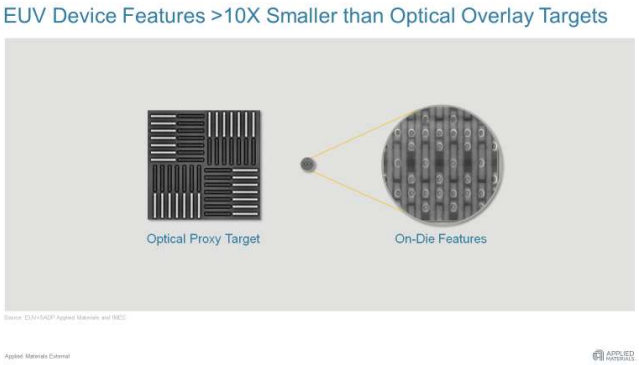
identifying and correcting the issues before they result in scrapped wafers. This data can also be used with our AIx platform, creating feedback loops that can help customers tune their process technologies.



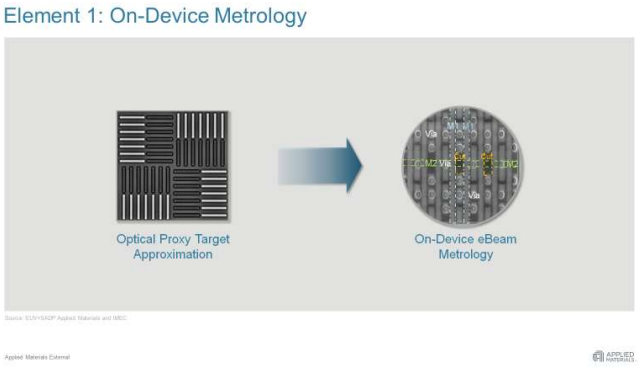
Finally, let's talk about the most critical challenge which is edge placement. Prior to EUV, edge placement was much easier. Features were larger, and if we aligned the optical scribe lines in the resist with the corresponding optical targets on the wafer, we could predict that the edges of the new features would be properly aligned with their opposite features on the previous layer. We could proceed one 2D layer at a time and make optical corrections along the way, producing uniform features from top to bottom. It's actually amazing that optical techniques have worked for so long.

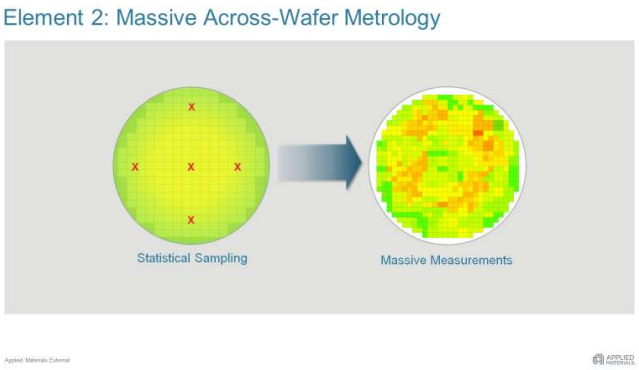
The optical proxy targets are at least 10 times larger than the features we are creating with EUV. Also, iterative process steps like multipatterning introduce variations, and 3D designs create stresses and interlayer distortions. Optical metrology and target-based approximation struggle to detect and diagnose these issues. As we continue to scale with EUV, engineers are encountering more situations where they are using all of the optical techniques properly and still having edge placement errors. They are hitting blind spots that bring scaling to a halt.

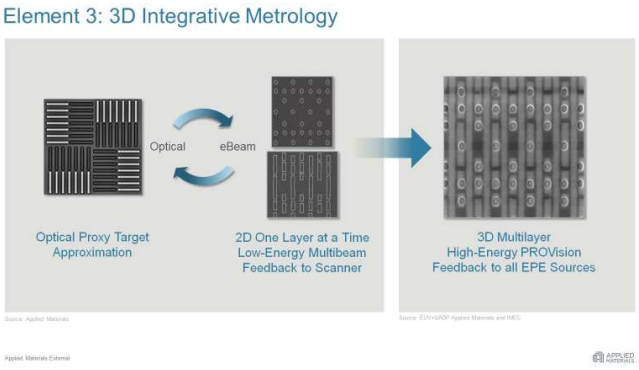
Today, most companies agree that we need to use eBeam metrology to complement optical metrology. But many of their efforts are still focused on diagnosing patterning failures one layer at a time and using the eBeam data to make optical corrections rather than solve the underlying process issues.



Applied is driving a different approach we call 3D patterning control. The approach is designed to overcome the blind spots by measuring and addressing all of the sources of edge placement error. The new 3D patterning control playbook has three elements. One, we supplement optical target approximation of patterns with actual, on device metrology using eBeam. Two, we supplement statistical sampling of a small number of locations with massive across-wafer metrology. And three, we go beyond 2D, one-layer at a time approaches to a 3D integrative approach that measures and addresses all of the critical layers as an integrated system.



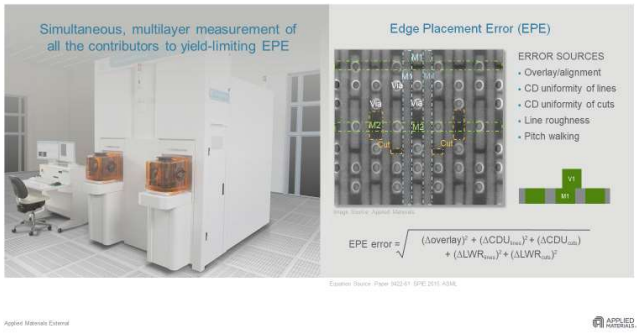




Applied's PROVision eBeam is specially designed for 3D patterning control. We use higher eBeam landing energies to penetrate the many layers of an advanced chip. Using our Elluminator technology,

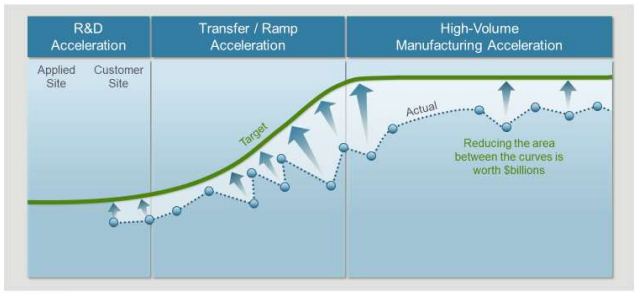
we capture the back-scattered electrons and produce high-contrast images of the many interdependent features. The clear, resulting images allow engineers to see and measure edge placement through all of the critical layers at the same time. PROVision measures all of the sources of edge placement errors, including overlay, CD uniformity, and line width roughness. It also gives engineers the data they need to refine process recipes for a wide range of equipment -- from litho to etch, deposition, anneals and CMP.

Applied PROVision 3E eBeam Metrology System



3D pattering control can be used at different times for different purposes. In early R&D, there are cases where eBeam metrology is the only way to develop a new process with correct edge placement. Later, eBeam data can help in the transition from R&D to tool matching and high-volume ramp. While customers will continue to use optical methods to keep their processes in spec during high-volume production, eBeam can help in quickly diagnosing and solving yield issues in HVM. If a manufacturer's optical control scheme has an excursion, it can take weeks to produce new masks with new proxy targets. Using actual, on-device measurement with eBeam, customers can continue to process wafers in the meantime.

eBeam Technology Helps Accelerate the "t" in PPACt



Finally, our customers have collaborated with us to present papers at SPIE, the industry's top lithography conference, showing how the new patterning control playbook can be used to achieve higher yields, faster. At last year's SPIE conference, Samsung and Applied demonstrated the use of eBeam SEM overlay and CD uniformity techniques to improve 3D edge placement and yield in logic devices. At the upcoming SPIE conference, Hynix and Applied will demonstrate similar edge placement

and yield improvements in DRAM. In addition, IBM and Applied will present a paper on the new VeritySEM technology for EUV photoresist metrology.

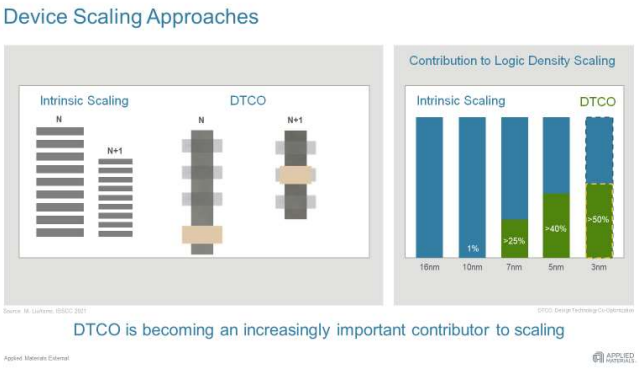
Thank you for listening, and now I'd like to hand the meeting over to Uday.

UDAY MITRA | Vice President, Semiconductors Products Group

Thank you, Ofer.

At the beginning of today's Master Class, Regina showed the two ways we can continue to shrink. One is intrinsic scaling, where feature size and pitch scaling increase density. The other is design technology co-optimization, or DTCO. Today, simply shrinking features creates major issues, such as an exponential increase in wiring resistance, and increases in leakage current which cannot be fixed by any lithographic process. As a result, DTCO is becoming a much larger contributor to the industry's scaling roadmap. When most of us think about Moore's Law, we remember the good old days of Dennard scaling, which worked until around the year 2000. Transistors were 2D, and we shrunk their sizes by 50% every two years.

We shrunk the gate that controls the on-off state of the transistor, and its length represented the node name: 130nm, 90nm, 65nm, and so on. We scaled the gate oxide proportionately. Dennard scaling gave us simultaneous improvements in performance, power and area-cost or PPAC.



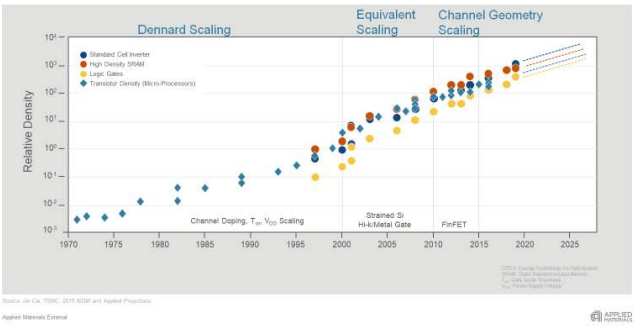
From around 2000 through 2010, gate and gate oxide scaling hit limits. We entered a period of equivalent scaling. The gate length stayed at around 30nm, and we used materials engineering to improve the performance and power. For example, we strained the silicon channel with epitaxy to increase performance. We switched from thin silicon dioxide gates to thicker high-K metal gates to reduce leakage and power consumption.

In around 2010, we moved to FinFETs, which marked a change from planar 2D transistors to 3D transistors. The FinFET's gates surrounded the transistor's electrical channel on 3 sides which enabled further improvements in performance and power. Typically three fins were used in each transistor to deliver enough current for fast operations within the logic cell. The logic cell is the minimum set of

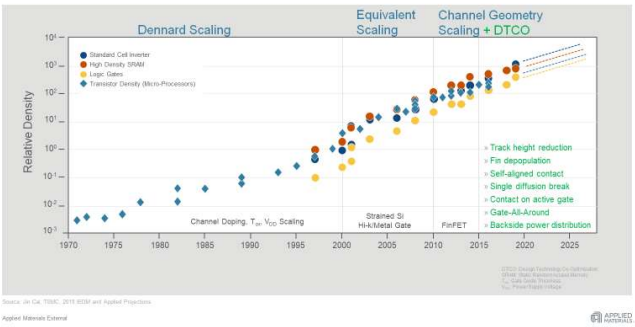
transistors and wiring needed to perform binary Boolean operations like add, subtract and compare. We need a positive and a negative transistor along with wiring for power and signals. Each cell requires isolation from neighboring cells. Today, we are in a new era where DTCO is driving as much as half of logic density scaling.

I'm going to explain two new ways to shrink using DTCO. One is the backside power distribution network, and another is Gate All Around transistors. I'll explain why the industry is moving to Gate All Around, and how these new transistors are made. Later, Raman will explain what these changes mean for Applied's business. It may seem counterintuitive to describe Gate All Around as a form of DTCO. But the goal of DTCO is to rearrange the layout of the logic cell in clever ways to increase density independent of the lithography pitch. And that's what Gate All Around helps us do. Gate All Around also enables higher performance and better performance-per-watt versus FinFET.

Next I'll provide some DTCO examples, beginning with some that are already in production.

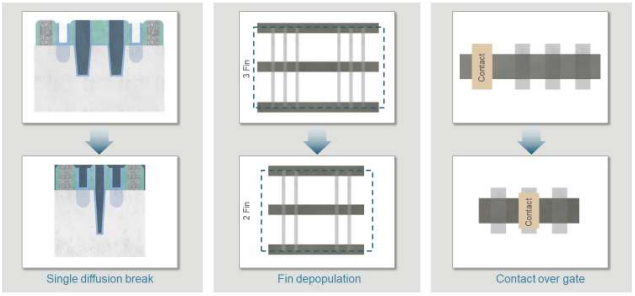


Logic Scaling Continues with DTCO Innovations



Here, we show the transition from double diffusion breaks, which isolate individual logic cells, to single diffusion breaks. The logic density advantage is obvious. Another example is fin depopulation. We raised the fin heights and improved the fin uniformity to increase the drive current, and this allowed us to reduce the number of fins per transistor from 3 to 2. A third example is contact over gate. Here, the gate contact to the logic cell is moved from the side of the fins to above the fins, thereby reducing the logic cell area.

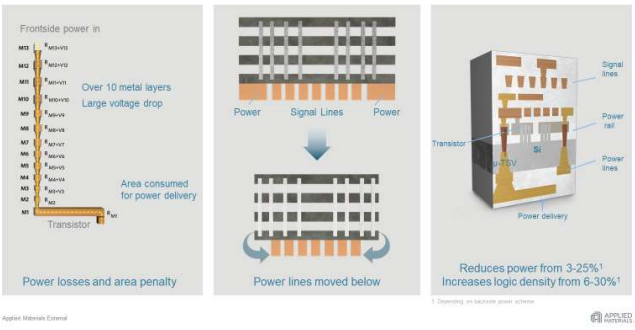
Cell Area Reduction Through DTCO



Now let's move to the emerging DTCO inflections. Customers are already talking about backside power distribution networks. Here is the general idea. Transistors and logic cells sit at the bottom of the wafer, and the power is routed from above. There are two kinds of wires: thick power lines, which provide the current needed for the transistors to switch, and thin signal lines, which help determine when to switch. All of this wiring proceeds through each metal layer of the chip, from top to bottom. At each metal layer of the chip, there is electrical resistance, and some of the supply voltage is lost. It is a bit like using a large number of extension cords to get the power from the source to the cell. It wastes power and creates heat.

So the emerging idea is to more efficiently route the thick power lines straight to the logic cells from the back side of the wafer. This approach explains the backside power naming convention. We believe Backside Power Distribution can reduce power consumption by as much as 25%. The DTCO benefit is an increase in logic density ranging from around 6% to 30%, depending on the approach. We'll go into more detail about how to engineer backside power distribution in our next Master Class on chip wiring and Advanced Packaging.

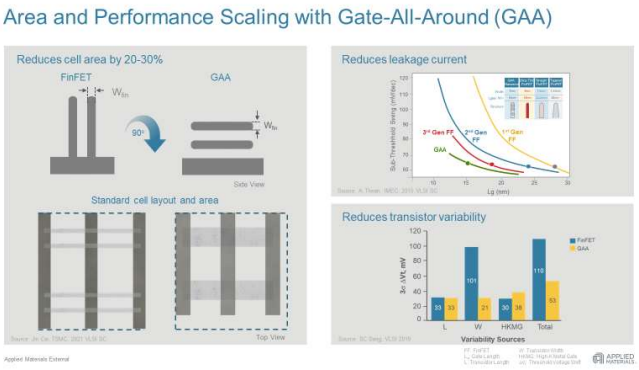
DTCO with Backside Power Distribution Network



Now let's dive into Gate All Around, which is one of the biggest and most important inflections since the FinFET. The industry will rearrange the elements of the transistor to increase density independent of the lithographic pitch. Pitch scaling may continue with Gate All Around, but it is unlikely to be very dramatic because we get scaling benefits from DTCO, and because further shrinking the transistor and wiring can create electrical challenges that negatively affect performance and power. Conceptually, Gate All Around is like lifting a FinFET transistor and rotating it by 90 degrees.

Instead of surrounding the channel on three sides as in FinFET, Gate All Around surrounds it on all four sides. The resulting channels are called nanowires, nanoribbons or nanosheets. I'll use nanosheets.

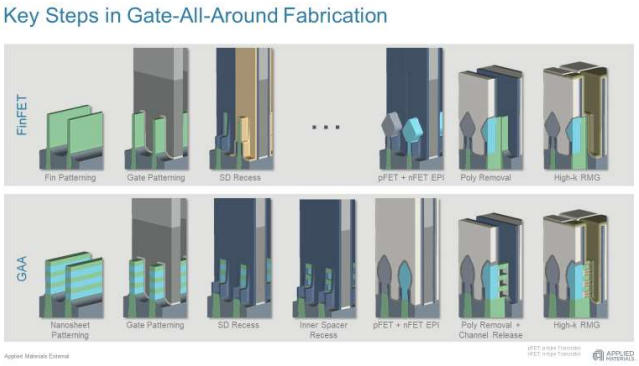
From a DTCO perspective, the approach allows us to shrink the logic cells in the X and Y dimensions. Designers have new choices. They might aggressively reduce area-cost while maintaining the performance of FinFETS. Or they might choose to widen the nanosheets to increase drive current -- thereby increasing performance by as much as 25% -- and increasing density by around 25% as well.



From a manufacturing perspective, Gate All Around borrows many of the proven processes used to make FinFETs, especially the ones that have a significant impact on performance and power. Selective epi is a prime example. There are also some critical new steps which I'll describe. I'll begin by describing how we create the channels, which is one of the key differences in Gate All Around versus FinFET. In FinFETs, the channel width is determined by lithography and etch. There tends to be variability, and this variability impacts performance and power.

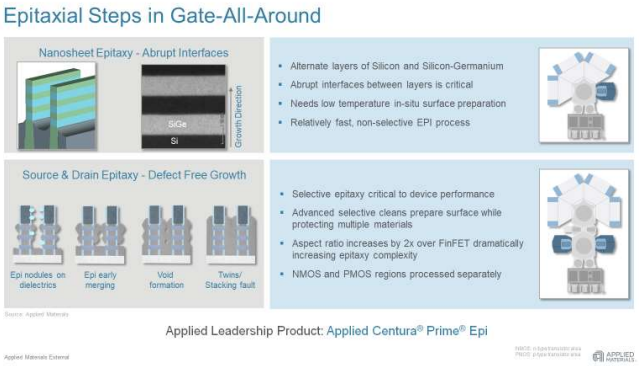
In Gate All Around, we deposit alternating layers of silicon and silicon germanium using simple, blanket epitaxy. These layers are etched to create individual rows of nanosheets. Next, shallow trenches are formed to isolate individual transistors, and a dummy gate is deposited. These processes are similar to those used in FinFETs. Then, the source and drain regions of the nanosheets are etched, forming a cavity. Next, the exposed silicon germanium in the channel region is selectively recessed, and the recess is filled with a dielectric spacer. The newly created inner spacer reduces parasitic capacitance between the transistor's gate and its contact. Then, the source and drain regions are etched to create cavities with optimized profiles.

These recesses are filled using a highly precise, selective epitaxy -- one material for the negative, NMOS region -- and another material for the positive, PMOS region. With the source and drain regions now completed, we move to the center region of the channel. The dummy gate is removed, which exposes the channel's superlattice. A highly selective process is used to remove the silicon germanium from the nanosheets, leaving behind freestanding silicon channels. The precision of epitaxy and selective materials removal is the key to uniform silicon channels with superior performance and power characteristics. To complete the transistors, we deposit a highly engineered gate oxide stack. And finally, we deposit an equally sophisticated metal gate stack. Together these elements control the drive current and the on-off state of the transistor.



Now that you have the overall Gate All Around process flow, I'll comment on some of the particular steps. Your heard about two uses of epitaxy. First was the alternating silicon and germanium blanket epi used to form the nanosheet super lattice. This is a simple, non-selective epi. Later, I described the two selective epi steps used in the source and drain regions of the PMOS and NMOS transistors. These are deposited using an integrated materials solution that combines a number of unique steps in one high-vacuum system.

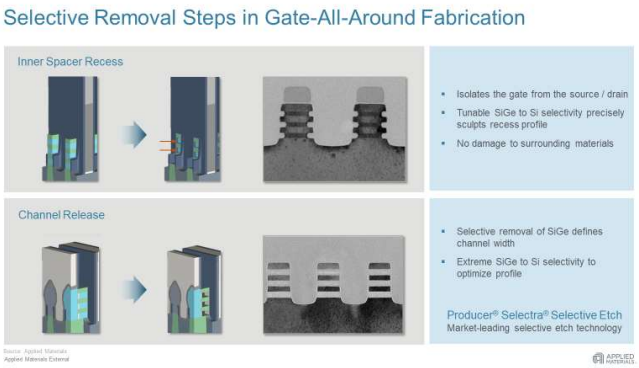
The sequence begins with interface cleaning and lateral silicon shaping that maximizes channel strain and increases electron mobility and performance. These are followed by selective epitaxy steps that precisely grow silicon through the very narrow features that were etched previously. This epitaxial source-drain engineering is slow, but critical to device performance.



There are also two new selective removal steps. First, we recessed the silicon germanium at the source-drain regions by around 5 to 10 nanometers to isolate the gate from the source-drain and reduce capacitance. These lateral recesses need to be uniform and square. Etch selectivity is important because the removal chemistry makes contact with the neighboring silicon, low-k spacers and shallow trench isolation oxide. A special challenge is ensuring a consistent silicon germanium recess across all of the structures being created. Applied has developed new metrology techniques that are co-optimized with the selective removal process to deliver precise recesses across the entire wafer. The second new step removes silicon germanium from the super-lattice and leaves the freestanding silicon nanosheets in place.

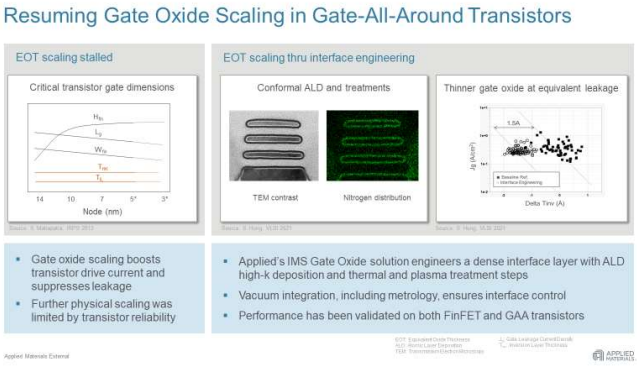
This is a very critical step because the width and uniformity of the nanosheets is key to transistor performance.

This is also one of the key differences between FinFET and Gate All Around: In FinFET, the channel width is defined by litho and etch, and it is difficult to control fin variability. Epitaxy is a slower and more precise process, and we can carefully engineer the channel width and uniformity. Applied's epitaxial deposition of the silicon and silicon germanium nanosheets results in very clean and clear interfaces. Our highly selective removal process removes the silicon germanium with extreme selectivity versus silicon.



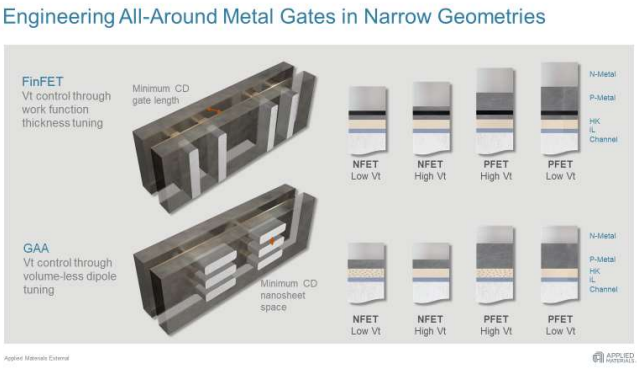
Next I'll discuss the gate dielectric, which is now undergoing a major change. The gate dielectric surrounds the channel, and it controls the transconductance which is the current voltage characteristics of the device. In the Dennard Scaling era I discussed earlier, the gate dielectric was scaled to smaller physical dimensions as measured by the gate oxide thickness. The scaling allowed us to reduce the supply voltage and still produce a fast on-off switch. In the equivalent scaling era, physical scaling of the gate oxide stalled. However, we continued to engineer improvements in gate dielectric properties and introduced a new metric, equivalent oxide thickness.

Over time, equivalent oxide thickness scaling also stalled, and it's remained stalled for more than 5 years. Today, Applied is sampling a new Integrated Materials Solution that's designed to allow equivalent oxide scaling to resume.Our solution works in high vacuum and combines ALD deposition with special plasma and thermal treatments along with in-situ metrology. Our approach thins the gate oxide by 1.5 angstroms and reduces leakage current by more than 10X. The solution has already been demonstrated to improve FinFET transistor performance, and it is now being evaluated for Gate-All-Around.



The last key materials engineering topic I'll address is the metal gate. Engineers tune their transistor designs with different threshold voltages to meet the performance-per-watt goals of specific computing markets, such as low-power mobile devices and high-performance servers. Metal ALD steps and treatments are used to help engineer these voltages, and the thickness of the metal layers is key. High demand for performance tuning, coupled with increases in complexity, has doubled the related process steps since the 16nm node. An untold story is that Applied has a strong market position in metal ALD. Our position is overlooked because our metal ALD chambers are integrated with our PVD platforms, and only our dielectric ALD revenue is reflected in third-party market reports.

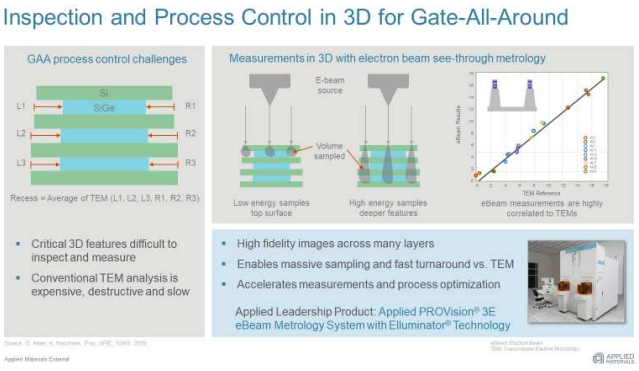
In gate-all-around, the metal gate engineering is more challenging because the space between the nanosheets is typically less than 10nm, which is less than the space available in FinFET designs. Our solutions for gate-all-around include dipole engineering of the dielectric layer which helps tune voltages without adding any volume. Next, we use ALD deposition in a high-vacuum, integrated materials solution to deposit the ultra-thin metal layers. Our integrated gate solution eliminates atmospheric contamination and enables us to precisely tune the transistor threshold voltages.



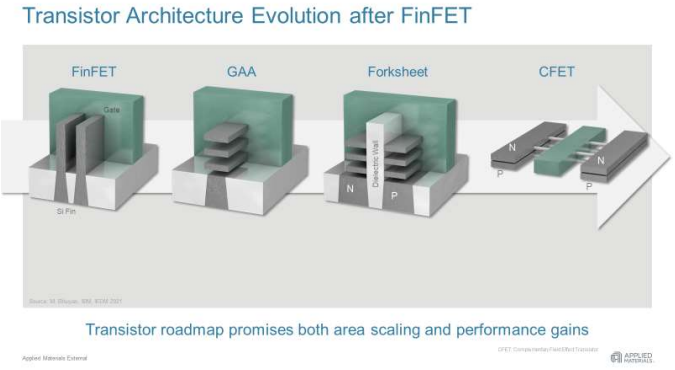
Finally, I'd like to say a word about process control in the Gate All Around regime. The 3D design techniques result in critical features becoming deeply buried within other structures, making them very difficult to measure, control and inspect. We can use transmission electron microscopy to assess our progress, but the technique is destructive and slow, and it doesn't provide the massive data we ideally need to quickly assess alternatives and progress. A key tool in the Gate All Around era will be technologies like Applied's PROVision eBeam metrology system which has our Elluminator technology.

This technology allows us to penetrate deep inside the many layers of the Gate All Around device and collect the back-scattered electrons to produce high-fidelity images and measurements. In fact, IMEC and Applied delivered a paper showing how PROVision can be used to control the Silicon Germanium recess step, which helps speed Gate All Around process development.

To accelerate R&D in the Gate All Around era, Applied will go far beyond unit process systems, delivering cooptimized systems, integrated materials solutions -- and AIx. With AIx, we can gather chamber sensor data, in-situ metrology data, and massive on-wafer metrology data – and then use analytics to converge on optimal solutions to these new engineering challenges.



I hope I've left you excited about the promise of DTCO, including the Backside Power Distribution Network and Gate All Around, which is coming even sooner. The progress won't end with Gate All Around. Engineers are already thinking about new ways to rearrange transistor and logic cell elements to continue to scale independent of the lithography pitch. One idea is forksheets, where a dielectric wall is inserted between the NMOS and PMOS transistors so they can be brought closer together. And further out, we can imagine complementary FETs, whereby the NMOS and PMOS transistors are stacked vertically.



Now, I'd like to hand the meeting over to Raman.

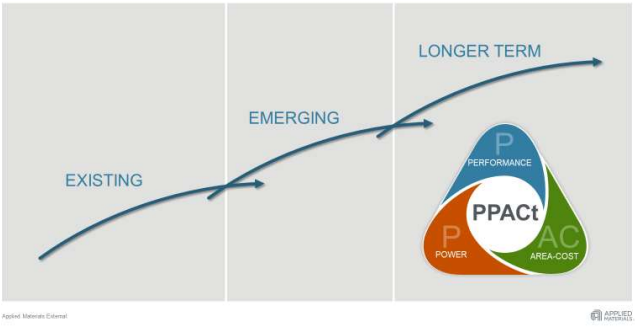
RAMAN ACHUTHARAMAN | Group Vice President , Semiconductor Products Group

Thanks Uday.

I hope you have enjoyed learning more about New Ways to Shrink, and the new ways Applied will accelerate the roadmap with new products and technologies. As Mike said during the intro, we also want to relate these changes to our revenue growth targets.

And that's what I will do today. In fact, some of these inflections are already generating revenue growth for us. Some will contribute more meaningfully between today and 2024, which is our financial target model horizon. And some will play out after 2024 and add to our longer-term growth opportunities.

Inflections Over Time



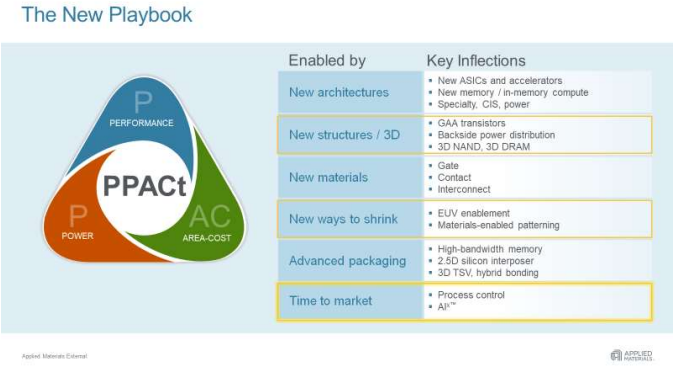
This is the 2024 financial model we introduced at our investor meeting last year which is derived from our strategic plan. WFE spending in calendar 2020 was $61 billion dollars. In our high scenario for 2024, WFE grows by around 63% versus 2020, reflecting annualized growth of around 13%.
In the same scenario, our goal is to nearly double our Semi Systems revenue, growing at around 18%, or about 1.5 times the rate of the market.

2024 Financial Model

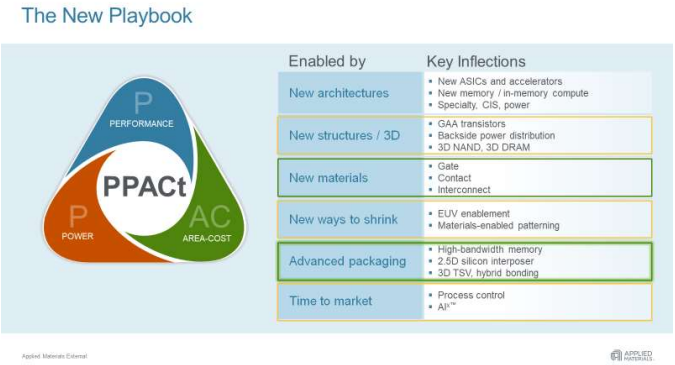
		FY'20	FY'24 MODEL		
			LOW	BASE	HIGH
	Revenue	$17.2B	$23.4B	$26.7B	$31.0B
	Semi Systems	$11.4B	$16.2B	$18.4B	$21.7B
	Services	$4.2B	$5.6B	$6.1B	$6.7B
	Display	$1.6B	$1.6B	$2.2B	$2.7B
NON-GAAP ADJUSTED	GM%	45.1%	47.5%	48.5%	48.8%
NON-GAAP ADJUSTED	OP%	26.3%	30.6%	32.4%	32.7%
NON-GAAP ADJUSTED	EPS	$4.17	$7.00	$8.50	$10.00

At the investor meeting, we shared that in 2020, over 55% of our Semi Systems revenue was in P-PAC-t enablement areas. Also, we said we expect to grow significantly faster in these areas through 2024.

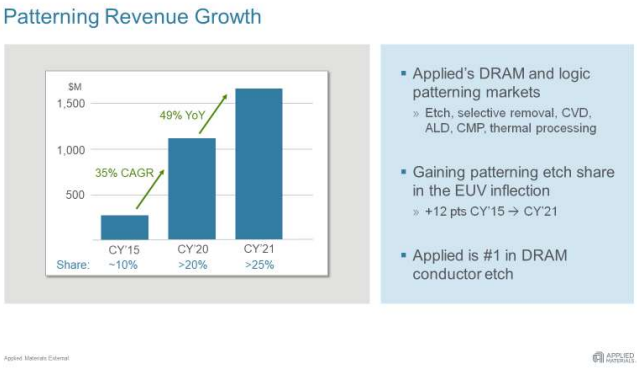
And that brings us to the 2022 Master Classes, where we are detailing the New Playbook inflections and the specific products and technologies that will generate this growth for Applied.
Today we talked about three areas of the New Playbook. Regina discussed New Ways to Shrink by enabling classic 2D scaling with EUV. Uday discussed new 3D structures like backside power distribution and Gate All Around that enable logic density improvements independent of lithography pitch. And Ofer described how we are accelerating R&D with eBeam and AIx. In a minute, I will show you how we expect to grow at nearly twice the rate of the market in all of these areas combined.



In our next Master Class, we'll go deeply into new materials, especially new wiring inflections that will overcome the resistance challenges that accompany EUV scaling. We'll show you how we expect to grow at three times the rate of the market in this area. In fact, wiring inflections should be the biggest growth driver for Applied between now and 2024. We'll also give you an update on heterogeneous design -- and heterogeneous integration using advanced packaging -- which helps the industry to advance all of the P-PACT-t vectors as Moore's Law slows.



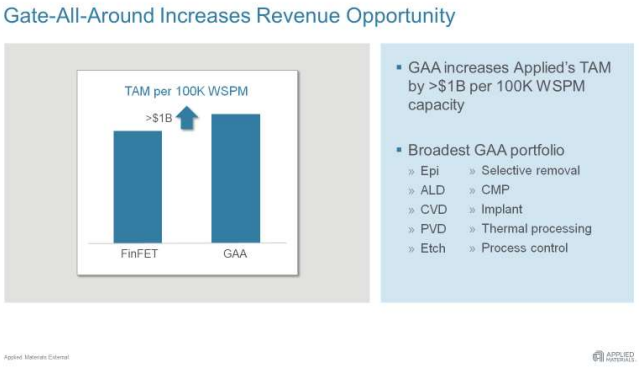
Now, let's take a deeper dive into the growth we're generating in the areas discussed in today's Master Class, beginning with Regina's topic of patterning. Our patterning opportunity is the sum of logic and DRAM customer spending for patterning steps in the process equipment markets we serve which include etch, CVD, CMP and thermal processes. Here you can see that we've grown at a 35% CAGR in patterning from 2015 through 2020, which is twice the rate of our markets, achieving $1 billion dollars in patterning revenue for the first time in 2020. In 2021, we grew by nearly 50% in patterning, outpacing our markets by more than 20 percentage points. We grew our patterning share from around 10% in 2015 to over 20% in 2020 and over 25% in 2021.



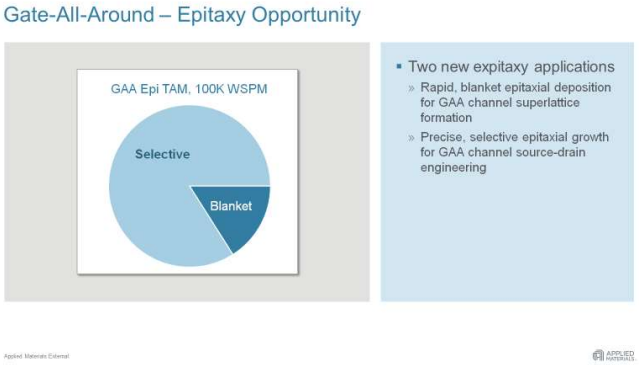
Most of our growth has been generated in CVD, which is our patterning films including Stensar for logic and Draco for DRAM, as well as in etch, which is our Sym3 product line. In fact, we've become number-one in DRAM conductor etch, and we've gaining strong etch share in the EUV inflection -- in both DRAM and logic. The new directional patterning technology Regina discussed is a longer-term growth driver.

Uday discussed Backside Power Distribution, which is also a longer-term inflection, and Gate All Around, which will begin to ramp by 2024 and grow significantly over the longer term. Gate All Around will increase Applied's market opportunity by more than $1 billion dollars per 100 thousand wafer starts of capacity. We expect to gain around 5 points of share in Gate All Around versus FinFET and capture the majority of the spending in our markets. Our Gate All Around opportunity includes 4 materials deposition technologies: PVD, CVD, ALD and epi. In materials removal, we offer etch, selective

removal and CMP. In materials modification, we participate in implant and thermals. The last area we compete in is process control.
No other company has this breadth, and our strategy is to combine our technologies in unique ways to give customers the best devices and the fastest time to market, including with the help of our AIx technology.

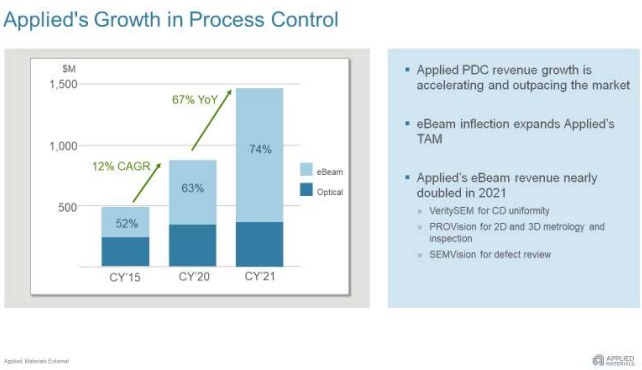


This chart summarizes the epi market in Gate All Around. There are two major applications, rapid blanket epi film deposition, and precise, selective epi growth. Applied's very first product was an epitaxy system, and we have been the strong number-one supplier ever since.

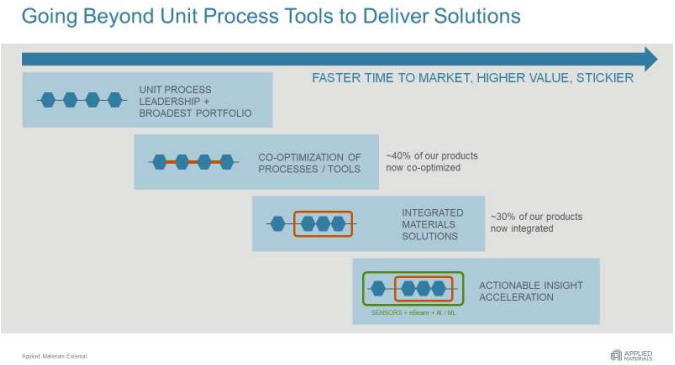


Turning to selective materials removal, this chart shows the growing adoption of this new technology in logic, from limited use at 14nm to growth in successive FinFET nodes and significant adoption in Gate All Around. Like selective epi, selective removal is critical to Gate All Around transistors because it helps control channel width and uniformity, which have a direct bearing on chip power and performance. Applied was first to deliver selective materials removal to the industry with our Selectra product, and we are the market leader by far with over 1,000 chambers in the field. We are capturing the majority of the selective etch positions in Gate All Around.

Process Control has been a significant growth driver for Applied over the past couple of years, and we expect to continue outgrowing the market as we address the limitations of optical metrology and accelerate time to market. We grew our PDC business by over 60% in calendar 2021, approaching $1.5 billion dollars in revenue. Ofer talked about our VeritySEM product for EUV photoresist inspection and process centering. We more than doubled our VeritySEM revenue in 2021. Ofer also discussed how EUV patterning and edge placement challenges are driving the need for massive across-the-wafer metrology -- and 3D metrology with PROVision. We nearly doubled our total eBeam revenue in 2021, surpassing $1 billion dollars.



In summary, Applied's strategy is to be the P-PAC-t enablement company for our customers. We will continue to pursue unit process leadership. But as the roadmap becomes increasingly complex, our strength is in our breadth and our ability to combine our technologies in unique ways to help our customers bring new processes and chips to market, faster. Increasingly, our revenue comes from cooptimized systems, and from Integrated Materials Solutions where we combine multiple technologies such as ALD, PVD and in-situ metrology in a single system, under high vacuum. We are already generating more than 70% of our Semi Systems revenue from these combinations. In the future, we will further accelerate the "t" in PPACt with co-optimized metrology and AIx.



I hope today's Master Class has given you insights into the roadmap challenges, technology inflections and unique solutions we are bringing to our customers. Some of these solutions are giving us growth today and through our 2024 model horizon, and a number of them will be adopted beyond 2024 and give us further opportunities to outperform the market. Now, I'd like join my colleagues for our Q&A session which will begin in a moment.