2024
PANEL DISCUSSION DURING IEDM

December 10, 2024 at 5:00PM PT
Hotel Nikko, San Francisco

Dr. Ian Cutress

Chief Analyst
More Than Moore

Dr. Ian Cutress is Chief Analyst at More Than Moore, a consulting firm working with leading semiconductor companies, and host of the popular YouTube channel TechTechPotato. As an influencer, Ian uses his extensive social platform for dedicated content on new technologies that meets the level of intrigue between customers, investors, enthusiasts, and a new generation. Prior to launching More Than Moore, Ian served for 11 years as Senior Editor at Anandtech.com, one of the top PC, smartphone, and semiconductor technology review websites on the internet, with a specialty in engineering-focused deep-dive analysis. Ian holds a doctorate degree in computational chemistry from the University of Oxford.

2024
PANEL DISCUSSION DURING IEDM

December 10, 2024 at 5:00PM PT
Hotel Nikko, San Francisco

Deepak Kulkarni

Senior Fellow
Advanced Technology Integration
Advanced Micro Devices

Deepak Kulkarni is currently a Senior Fellow at Advanced Micro Devices (AMD), where he leads the Advanced Technology Integration team. In his role, Deepak is responsible for designing and developing innovative packaging technologies across AMD’s extensive product portfolio, which includes Central Processing Units (CPUs), Graphics Processing Units (GPUs), and Artificial Intelligence (AI) accelerators.

With 19 years of experience in packaging, Deepak has overseen the development of several industry-leading innovations, including panel-level fan-out, Embedded Multi-die Interconnect Bridge (EMIB), Elevated Fan-Out Bridge (EFB), and 3.5D packaging solutions. Prior to his tenure at AMD, he served as Senior Director at Intel Corporation. Deepak earned his PhD in Mechanical Engineering with a minor in Computational Science from the University of Illinois at Urbana-Champaign.

2024
PANEL DISCUSSION DURING IEDM

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Johanna Swan

Intel Fellow and Director
Package Research and Systems Solutions
Intel Corporation

Johanna Swan is an Intel Fellow and the Director of Package Research and Systems Solutions at Intel Foundry Technology Development. An expert in advanced electronic packaging, Swan began her Intel career in 2000, focusing initially on packaging solutions for wireless, cellular and memory products followed by packaging for logic and 3D heterogeneous integration. Prior to Intel, Swan spent 16 years at Lawrence Livermore National Lab.

Kam Kittrell

Vice President of Product Management
Digital and Signoff Group
Cadence

Kam Kittrell has 35 years of experience in various IC design engineering, engineering management and marketing roles. He is currently the VP of product management in Cadence’s Digital and Signoff Group which covers the digital design EDA tool suite from System C through implementation and signoff. His portfolio also includes Cadence’s Integrity 3DIC platform to perform 3DIC early prototype, chiplet/substrate/interposer implementation, electrical and physical signoff, as well as analysis of power integrity, signal integrity, and thermal effects.

2024
PANEL DISCUSSION DURING IEDM

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Terrance (Terry) Lee

Vice President and General Manager
Heterogeneous Integration
Applied Materials

Terry Lee is the General Manager for the Heterogeneous Integration Business Unit. He is responsible for building and growing the advanced packaging business for Applied Materials. Previously, he worked in Etch, Dielectric Deposition, Chemical Mechanical Planarization and Plating Business Units. Before joining Applied Materials, he held executive positions in Business Development and Finance in the capital equipment sector. Mr. Lee earned a Bachelor of Science degree in Chemical Engineering from UC Berkeley and holds patents in CVD, CMP and Etch.