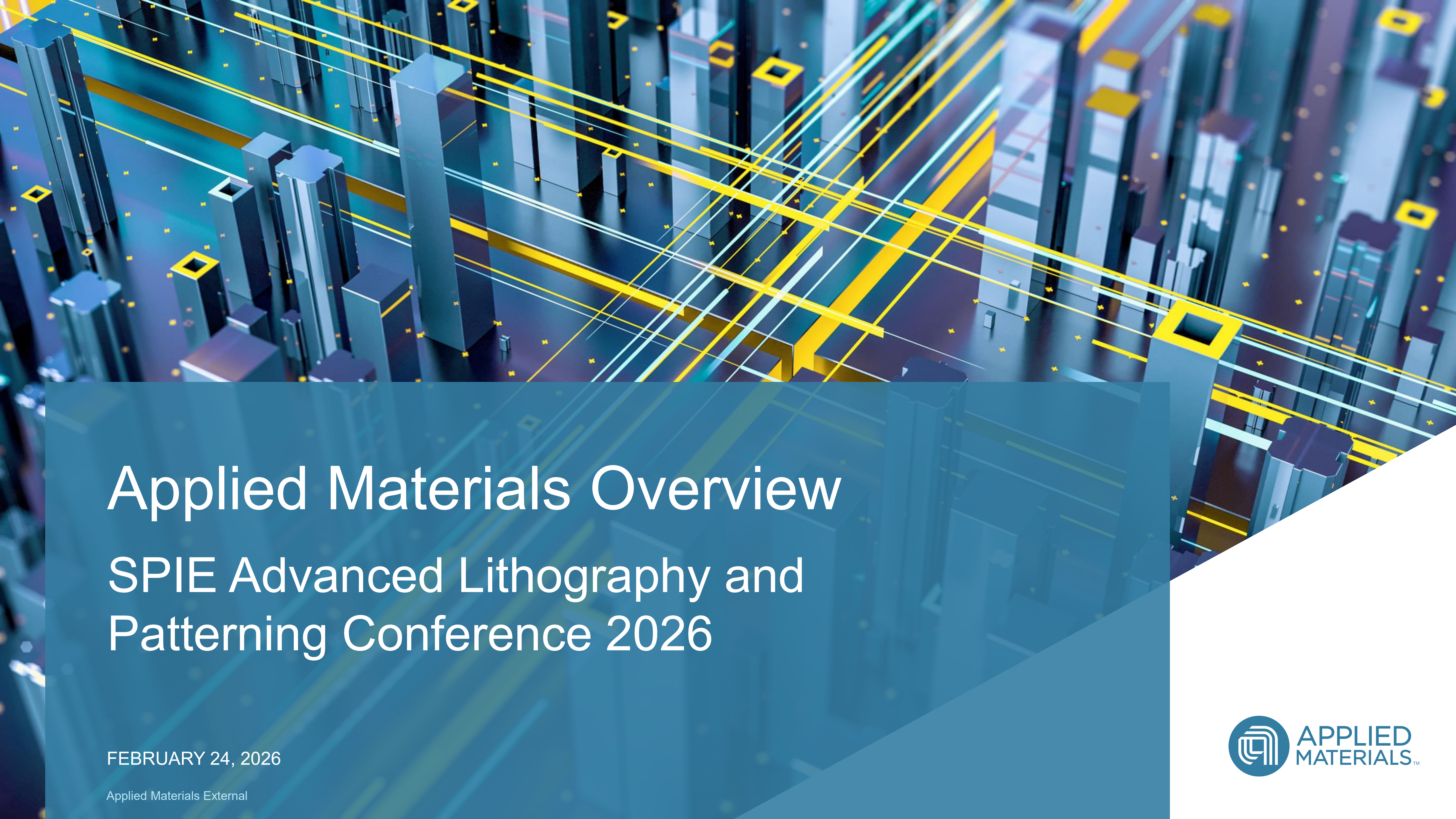


# Applied Materials Overview

## SPIE Advanced Lithography and Patterning Conference 2026

FEBRUARY 24, 2026

# Forward-Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our capital allocation and cash deployment strategies, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic, political and industry conditions, including changes in interest rates and prices for goods and services; the implementation of additional export regulations and license requirements and their interpretation, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies and our ability to obtain licenses or authorizations on a timely basis, if at all; imposition of new or increases in tariffs and any retaliatory measures, including their impact on demand for our products and services; our ability to effectively mitigate the impact of tariffs; the effects of geopolitical turmoil or conflicts; demand for semiconductor chips and electronic devices; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; cybersecurity incidents affecting our information systems or information contained in them, or affecting our operations, suppliers, customers or vendors; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the effects of regional or global health epidemics; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our filings with the Securities and Exchange Commission, including our most recent Forms 10-K, 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

# AGENDA

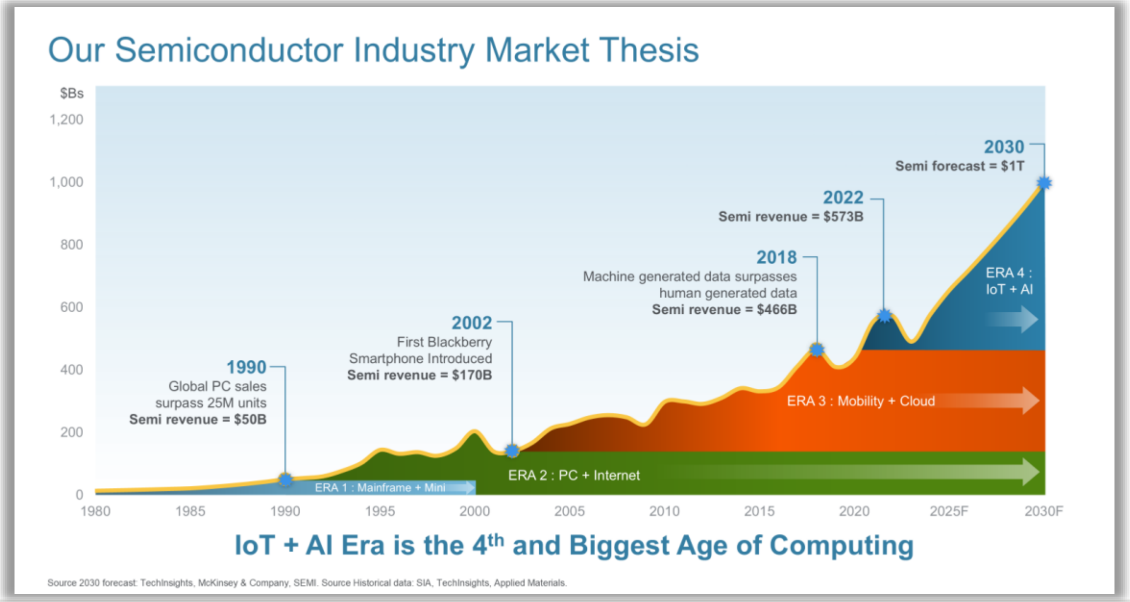
- Market Outlook
- Materials Engineering Markets
- New Product Introductions
- Inflection-Focused Innovation
- Q&A

# KEY MESSAGES

1. $1T semi industry is arriving several years earlier than prior forecasts
2. WFE industry mix is shifting to leading-edge F/L, DRAM and packaging
3. Materials engineering is increasingly key to roadmap inflections
4. Applied is ramping new systems that enable high-performance computing
5. Inflection-focused innovation creates value for customers and Applied

# Prior View of Semi and WFE Markets

Semiconductor revenues to reach $1 trillion by 2030



## Our Semiconductor Industry Market Thesis

**IoT + AI Era is the 4th and Biggest Age of Computing**

Source 2030 forecast: TechInsights, McKinsey & Company, SEMI. Source Historical data: SIA, TechInsights, Applied Materials.

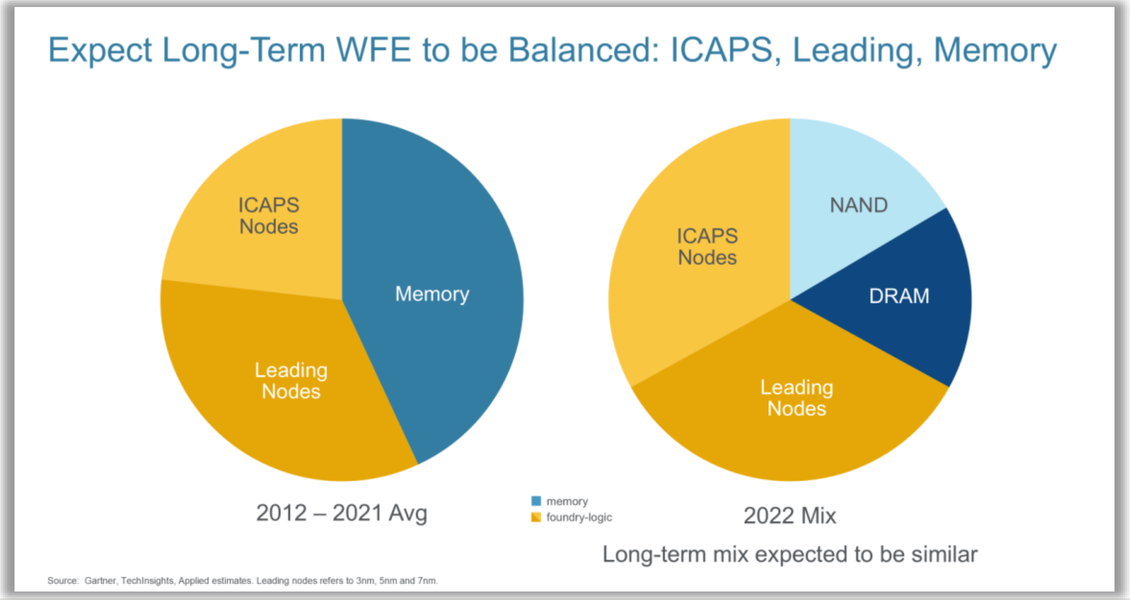
Update:

*"With the accelerated growth of AI end markets, we believe that global semiconductor industry revenues can potentially reach* ***$1 trillion in 2026****, several years earlier than prior predictions.*

\- *CEO Earnings Commentary, Feb. 12, 2026*

WFE mix expected to be:

- 1/3 leading-edge foundry/logic
- 1/3 ICAPS foundry/logic
- 1/3 memory, evenly split between DRAM and NAND



## Expect Long-Term WFE to be Balanced: ICAPS, Leading, Memory

Long-term mix expected to be similar

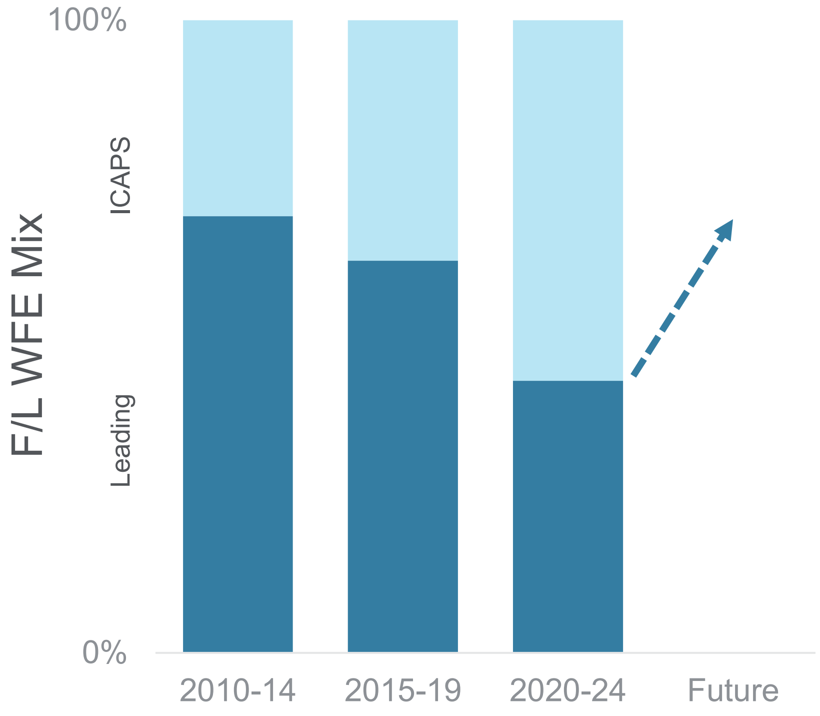
Source: Gartner, TechInsights, Applied estimates. Leading nodes refers to 3nm, 5nm and 7nm.

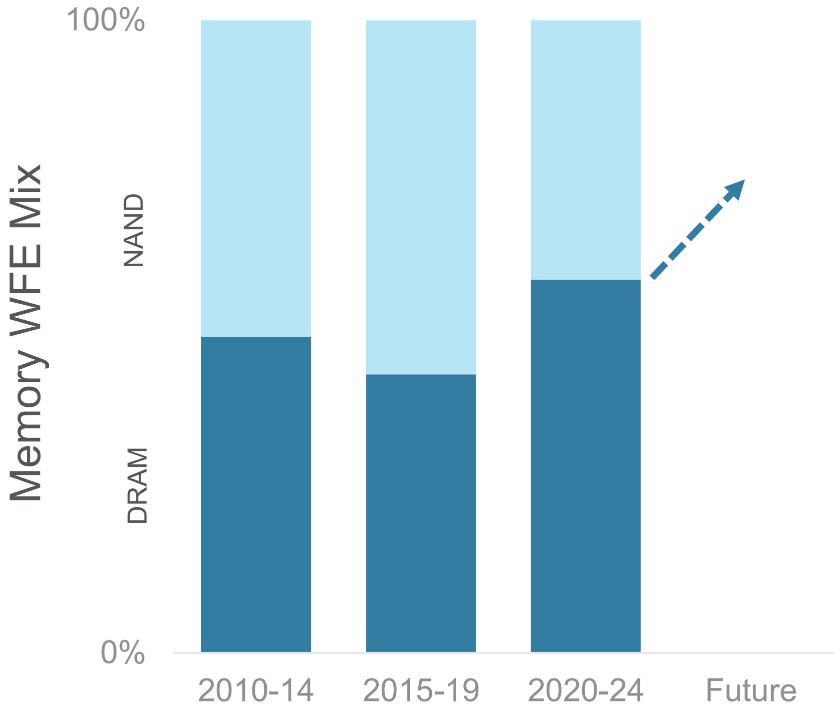
Update:

*"Today, the most critical and* ***fastest growing markets*** *are leading-edge, high-bandwidth memory DRAM, and advanced packaging."*

\- *CEO Earnings Commentary, Feb. 12, 2026*

# WFE Spending Mix is Changing





2020-24:

- Strong ICAPS WFE driven by IoT, EV/AV and global investments in geographically secure supply chains

2025+:

- Data center AI driving strong leading-edge F/L WFE
- Expect moderate ICAPS WFE growth after digestion period

2015-19:

- NAND led memory WFE in the conversion from 2D to 3D architectures which required greenfield spending

2025+:

- Data center AI driving strong DRAM and HBM WFE
- Expect NAND to be <10% of WFE as technology transitions satisfy the majority of bit demand growth

ICAPS = IoT, Communications, Auto, Power, Sensors. EV/AV = electric and autonomous vehicles.
Leading-edge = 7nm and smaller (2018+); three leading nodes (prior to 2018).

Source: Applied Materials estimates

# 2026 WFE Market Outlook

## FASTEST GROWING AREAS OF THE MARKET

| | INFLECTIONS | 2026 WFE MARKET DRIVERS |
|---|---|---|
| **Leading-Edge Foundry/Logic** | Gate-all-around transistors<br>Backside power delivery | FinFET capacity additions<br>GAA nodes ramping |
| **DRAM** | $4F^2$<br>3D DRAM | $6F^2$ capacity additions, incl HBM<br>R&D on next-generation inflections |
| **Advanced Packaging** | High-bandwidth memory (HBM)<br>Hybrid bonding<br>Panel substrates | HBM packaging<br>3D chiplet stacking |

**APPLIED MATERIALS**

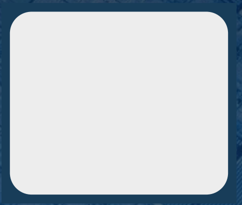
**#1** Process Equipment Company in All Three Markets

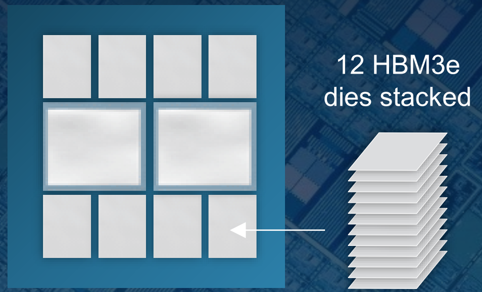
## OTHER AREAS

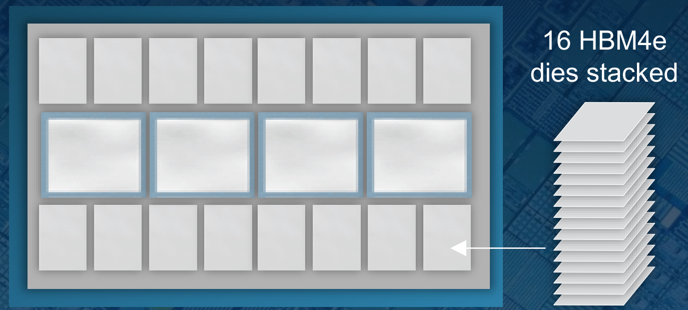
| | | |
|---|---|---|
| **NAND** | Increased layers, technology transitions | Modest growth<br>Expect to remain <10% of WFE |
| **ICAPS** | Compound semi (SiC, GaN)<br>Photonics | ~Flat, globally and in China |

ICAPS = IoT, Communications, Auto, Power, Sensors; represents nodes 10nm and larger

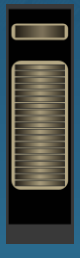
# SILICON CONTENT RAPIDLY GROWING

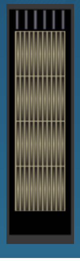






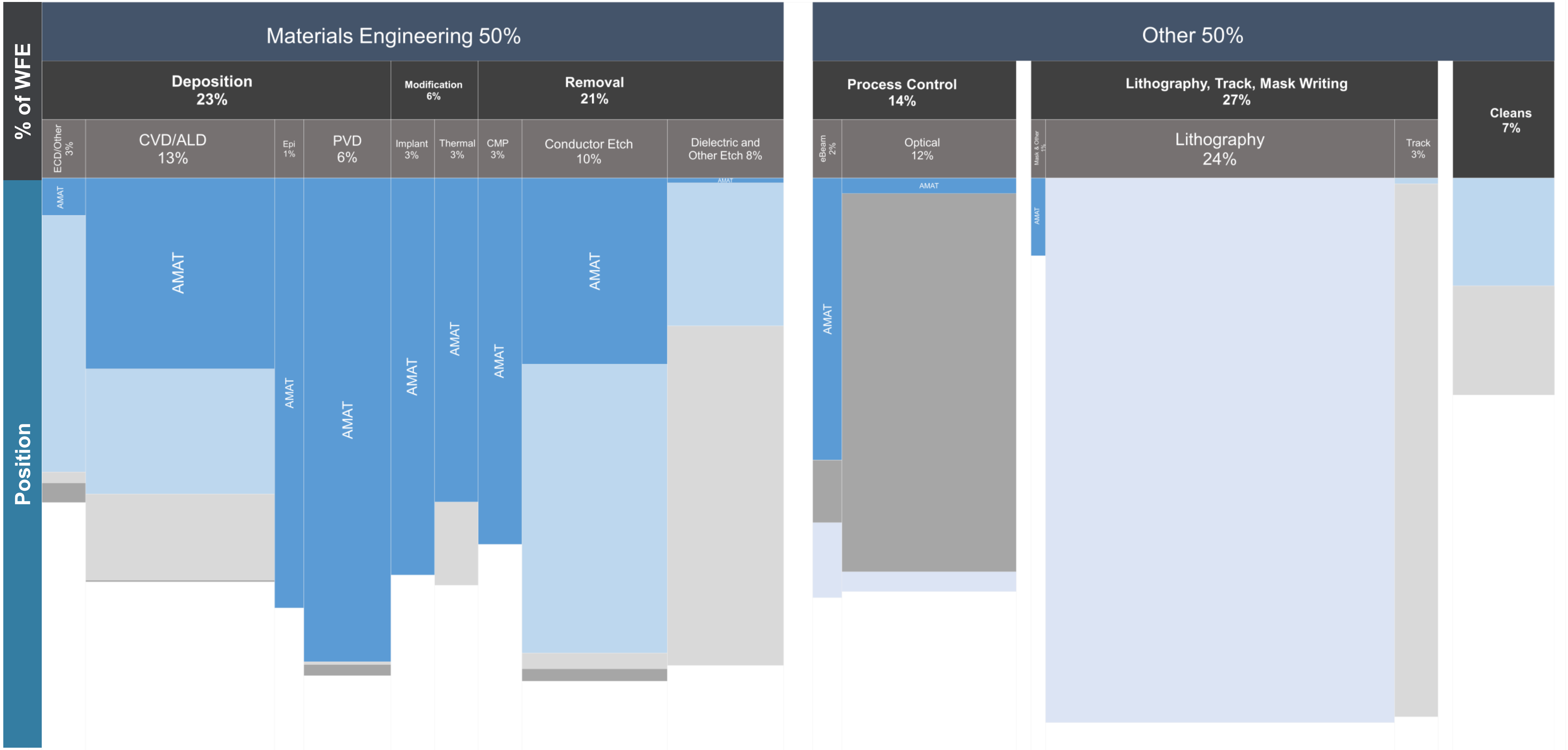
| | CPU<br>2020 | GPU<br>2025 | Future GPU<br>2027 |
|---|---|---|---|
| Logic node | 10nm | 4nm | 3nm |
| Transistors per logic die | 10B | >200B | >300B |
| Wiring (logic + HBMs) | 50 miles | >800 miles | >2,000 miles |
| Die count (logic + HBMs) | 1 | >100 | >300 |
| HBM stacks / dies per stack | | 8 / 12 | 16 / 16 |
| GPU/HBM wafers per system | | Normalized to 1X | GPUs ~4X<br>HBMs ~9X |





Source: Applied Materials estimates; NVIDIA roadmap

# 2024 WFE ($103B) by Technology – Materials Engineering 50%



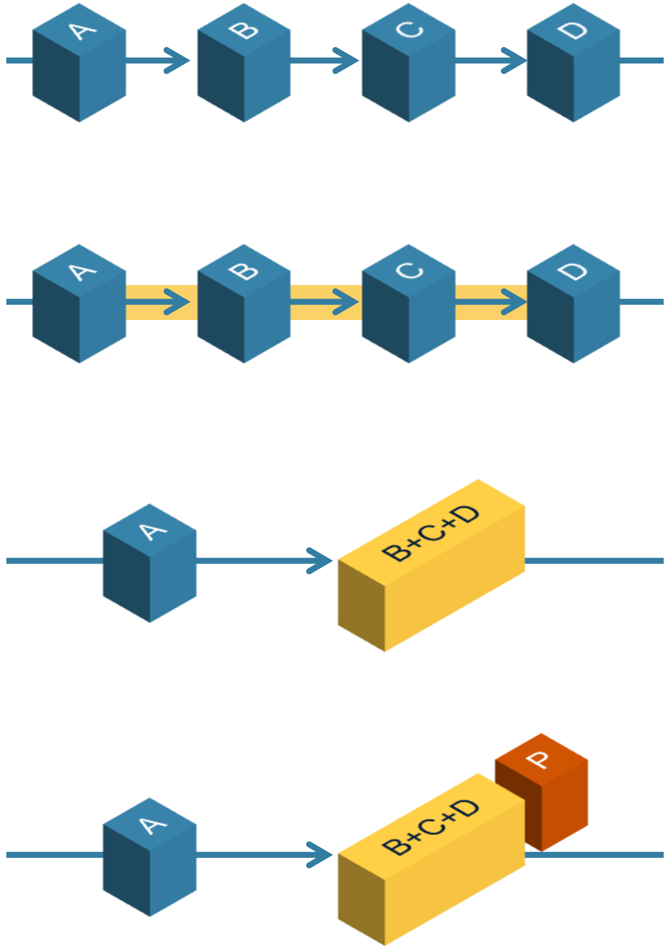
Source: TechInsights, released April 2025. Wafer Fabrication Equipment (WFE) = front end WFE and excludes “other WFE” of $3.4B.

# Applied's Unique Portfolio: Connecting Technologies

## BROADEST CAPABILITIES

| | | **Applied** | **Competitors** | | | | |
|---|---|---|---|---|---|---|---|
| | ALD | ✓ | ✓ | | | ✓ | ✓ |
| | Bonding | **partner** | | | | | ✓ |
| | Cleans | **partner** | | | | ✓ | ✓ |
| **#1** | CMP | ✓ | | | | | |
| **#1** | CVD | ✓ | ✓ | | ✓ | ✓ | ✓ |
| | ECD | ✓ | | | | ✓ | |
| **#1** | Epitaxy | ✓ | ✓ | | | | |
| | Etch | ✓ | | | ✓ | ✓ | ✓ |
| | Furnace | **partner** | | | | | ✓ |
| **#1** | Implant | ✓ | | | | | |
| | Lithography | **partner** | | ✓ | | | |
| | M&I (optical) | ✓ | | | ✓ | | |
| **#1** | M&I (e-beam) | ✓ | | ✓ | ✓ | | |
| **#1** | PVD | ✓ | | | ✓ | | |
| **#1** | Thermal | ✓ | | | | | ✓ |
| | Track | | | | | | ✓ |

## UNIQUE COMBINATIONS



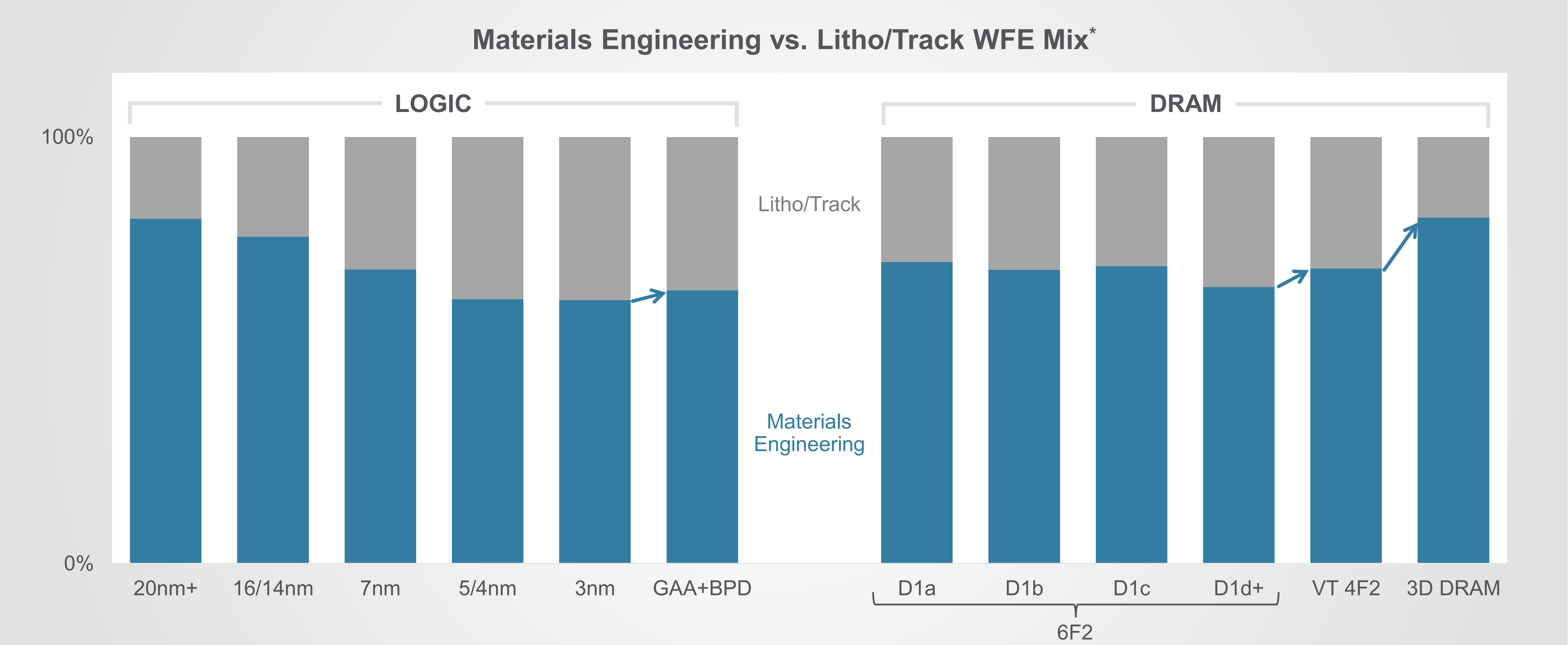
Unit Process Tools

Co-optimized Solutions

Integrated Materials Solutions (IMS™)

**Connected with Partners**

# Expect Materials Engineering to Increase within WFE Mix



| | 20nm+ | 16/14nm | 7nm | 5/4nm | 3nm | GAA+BPD | D1a | D1b | D1c | D1d+ | VT 4F2 | 3D DRAM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Materials engr % of **incremental** WFE* | | **>50%** | **>40%** | **>40%** | **>60%** | **>75%** | | **>50%** | **>70%** | **>30%** | **>100%** | **>100%** |

Source: Applied Materials analysis

* Materials engineering vs litho/track WFE mix & ME as % of incremental WFE exclude cleans and process control

Materials engineering (ME) % of incremental WFE = (ME WFE spend on new node – ME WFE spend on prior node) / (WFE spend on new node – WFE spend on prior node)

# Recently Launched Products for Energy-Efficient HPC

**OCT 2025**


LE F/L
DRAM

**Xtera™ Epi**

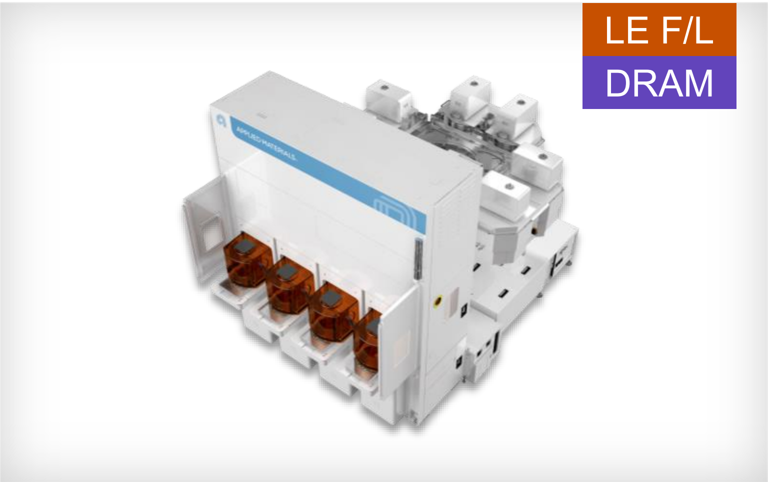

LE F/L
DRAM

**PROVision™ 10 eBeam Metrology**


ADV. PKG

**Kinex™ Integrated Die-to-Wafer Hybrid Bonding System**

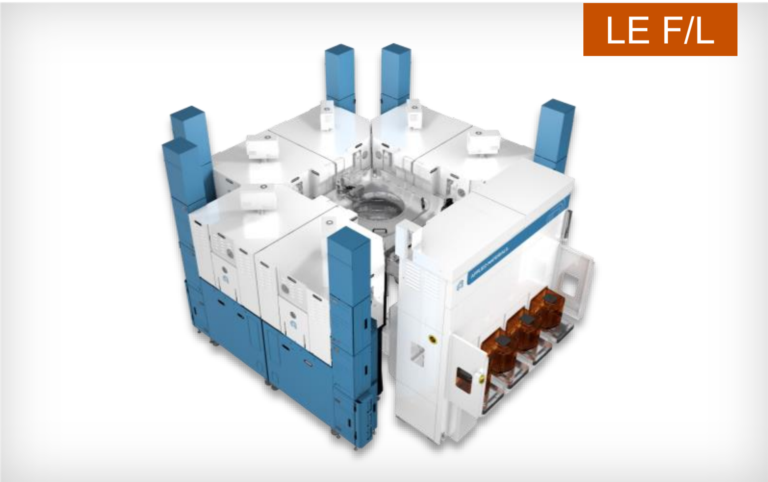
**FEB 2026**


LE F/L
DRAM

**Viva™ Radical Treatment**

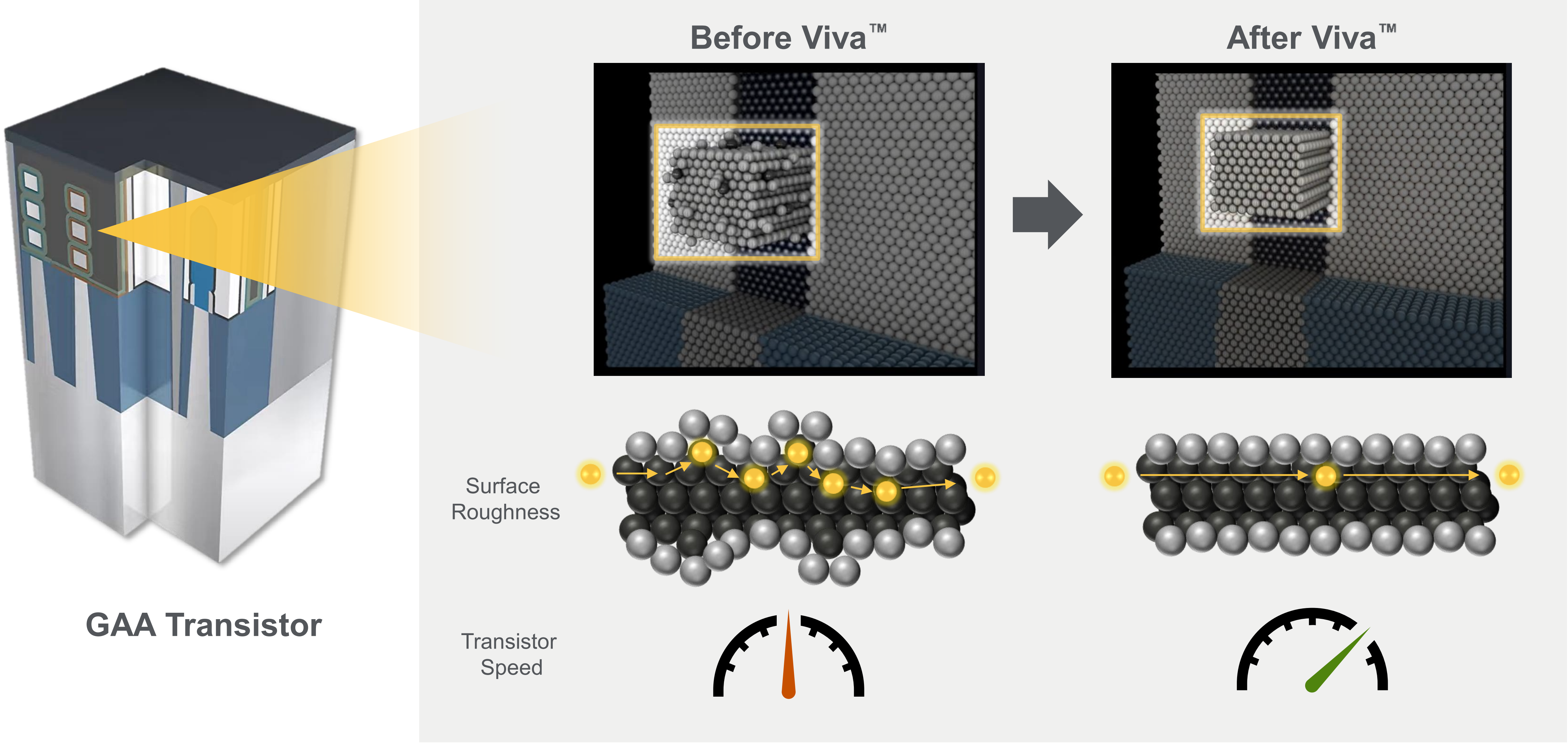

LE F/L
DRAM

**Sym3™ Z Magnum™ Etch**


LE F/L

**Spectral™ Moly ALD**

# GAA Nanosheet Channels Demand Angstrom-Level Treatments



**Before Viva™**

**After Viva™**

Surface Roughness

Transistor Speed

**GAA Transistor**

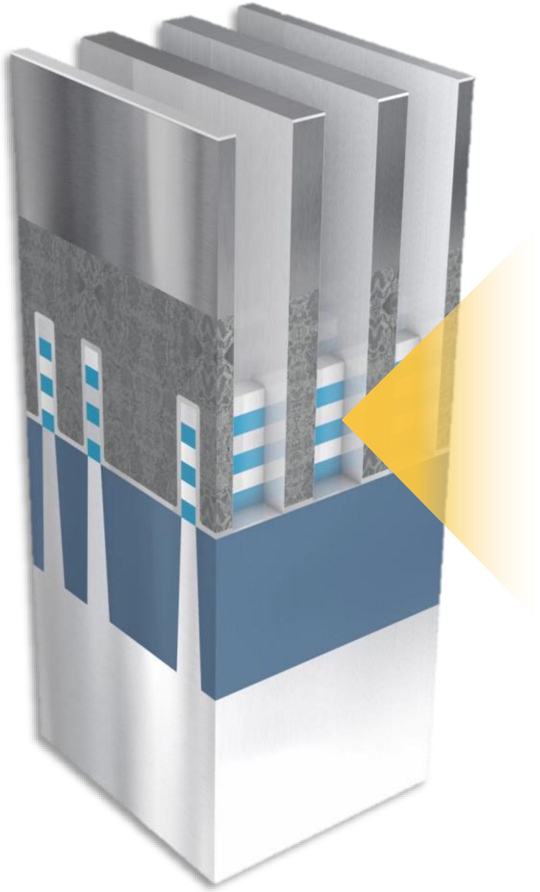
# Applied Producer™ Viva™ Radical Treatment

Gentle, damage-free, conformal nanosheet channel treatment

- ✓ Nanosheet smoothing with angstrom-level control
- ✓ Maintain nanosheet channel integrity
- ✓ Remove surface impurities and defects
- ✓ Increase transistor speed and chip performance

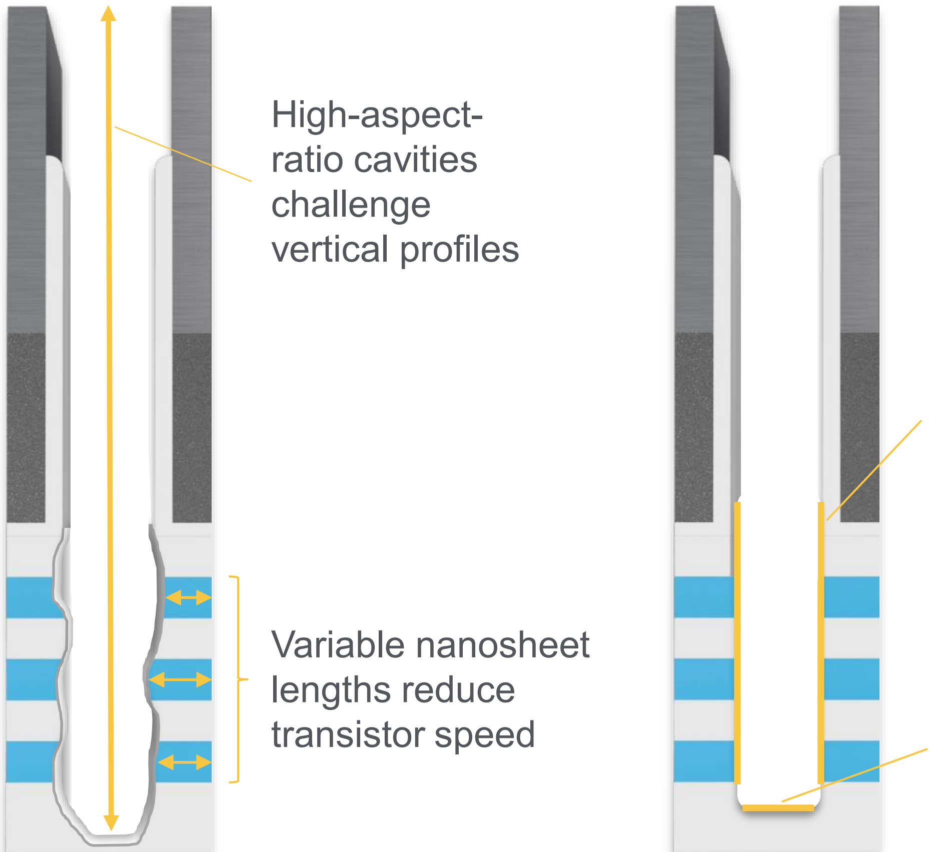
Adopted by leading-edge F/L customers at 2nm and beyond process nodes

# GAA Source and Drain Cavity-Shaping Challenges



GAA Transistor

## Etching Source & Drain Cavities



High-aspect-ratio cavities challenge vertical profiles

Variable nanosheet lengths reduce transistor speed

Vertical “walls” produce uniform nanosheet lengths for faster transistors

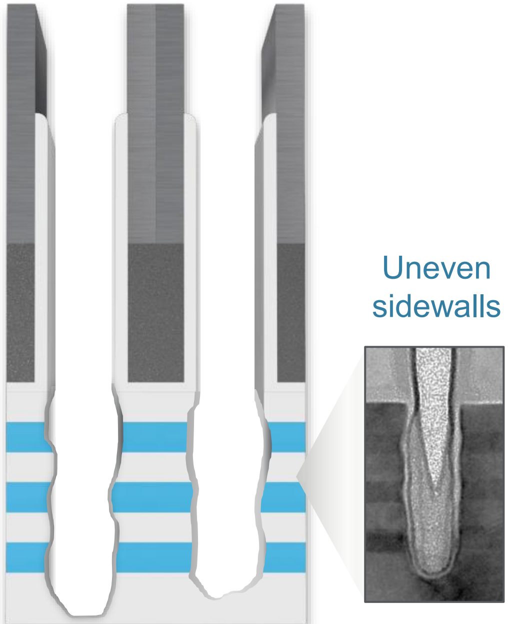
Flat rectangular “floors” promote void-free epi growth and increase epi-nanosheet contact for faster transistors

Non-Ideal

Ideal

# Second-Generation Pulsed Voltage Technology (PVT2)

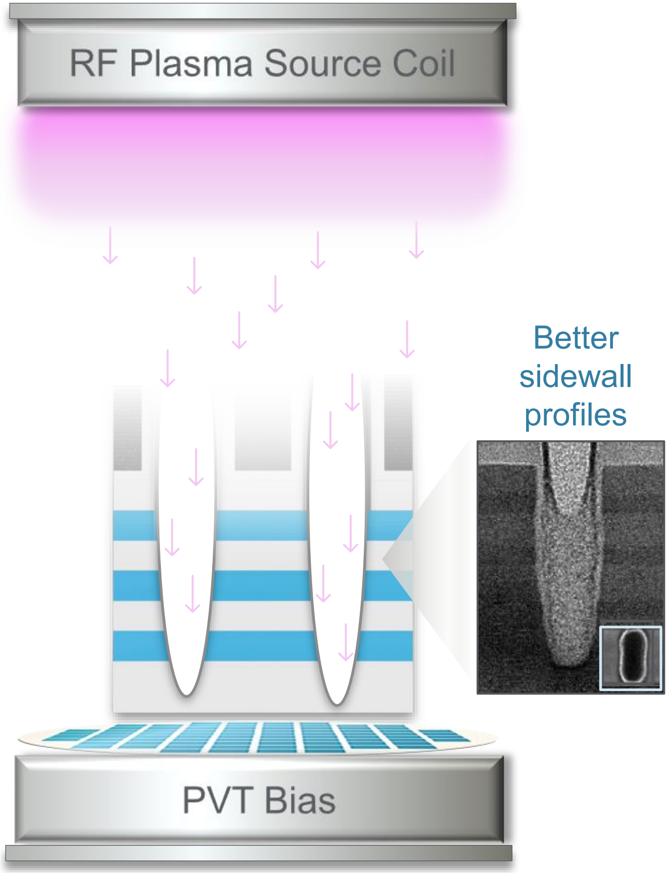
### GAA Etch Challenge without PVT


Uneven sidewalls

Depth variation

### Sym3™ Z with PVT

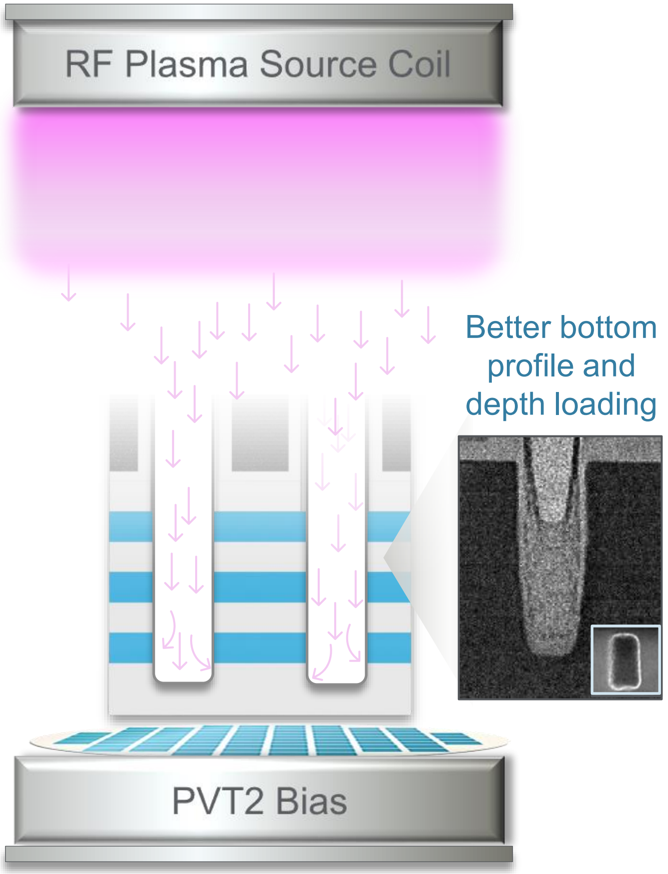
for ≥2nm nodes



Better sidewall profiles

### Sym3™ Z Magnum™ with PVT2

for ≤2nm nodes



Better bottom profile and depth loading

## PVT2 shapes better profiles in high-aspect-ratio structures

# Applied Centris™ Sym3™ Z and Sym3™ Z Magnum™ Etch

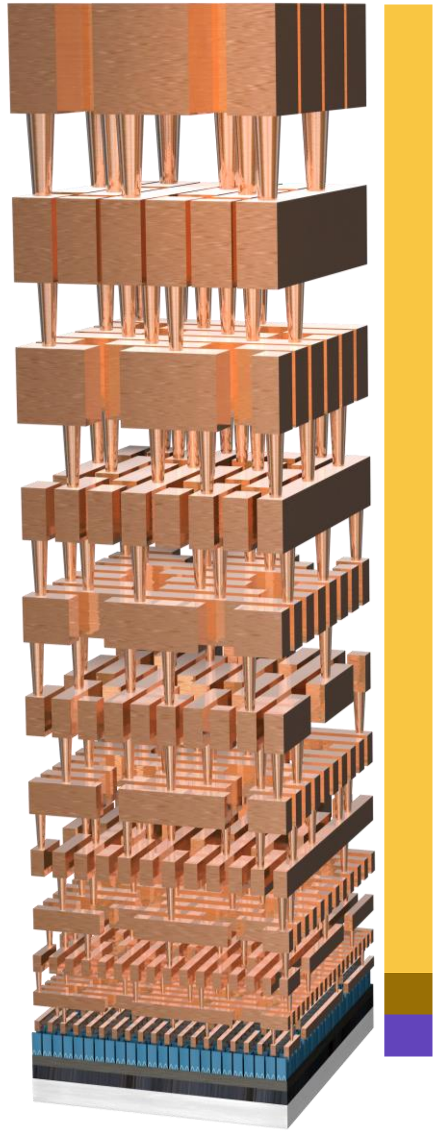
## GAA source and drain cavity shaping & DRAM critical silicon etching

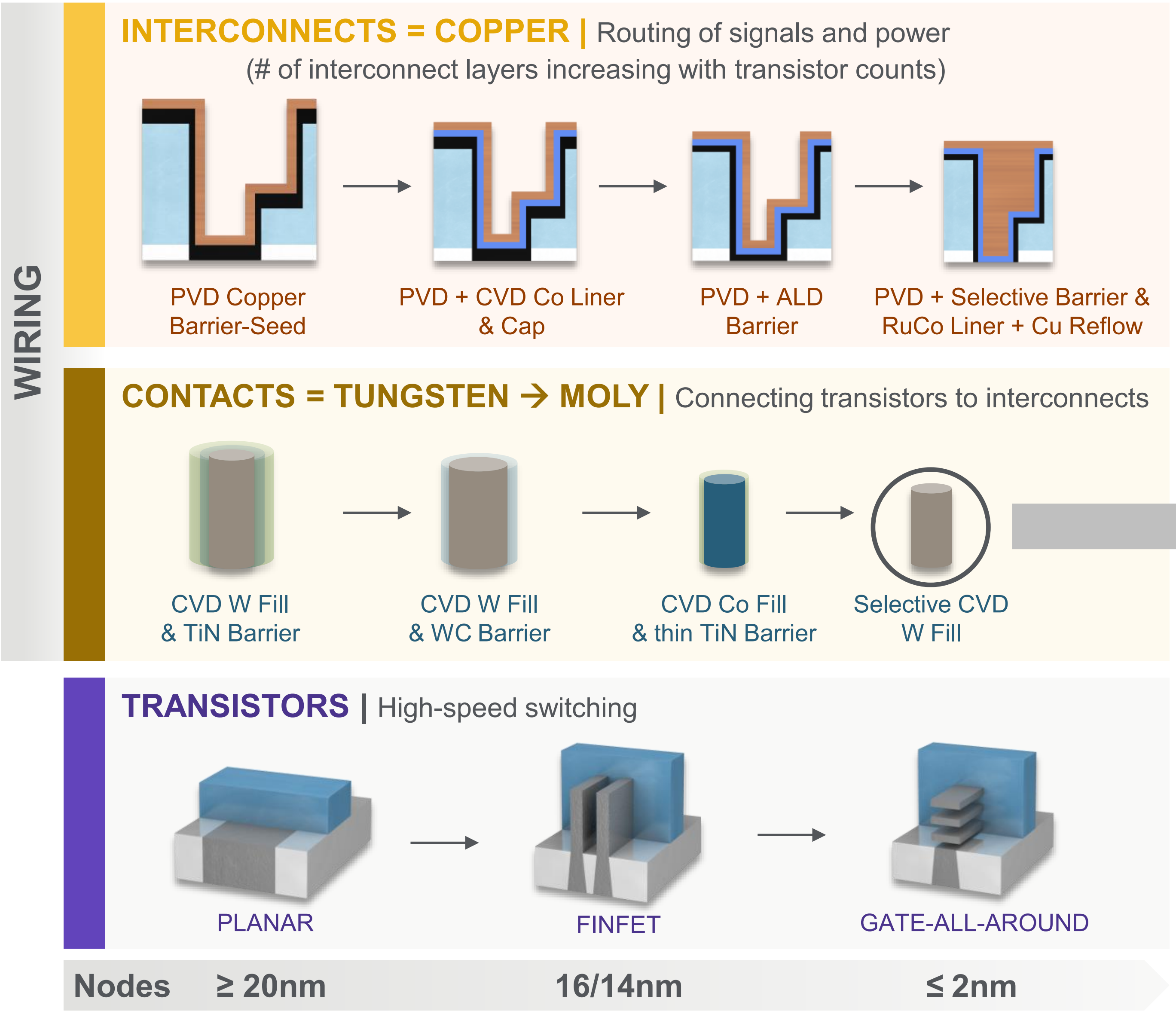
- ✓ Vertical and even sidewalls
- ✓ Best-in-class square-bottom shaping capabilities
- ✓ High etch-depth uniformity (depth loading)
- ✓ Increased device yield

Adopted at leading-edge F/L and DRAM customers

Extends #1 conductor etch position in leading-edge F/L and DRAM

# Wiring: Advanced Foundry-Logic Architecture





**INTERCONNECTS = COPPER |** Routing of signals and power
(# of interconnect layers increasing with transistor counts)

PVD Copper Barrier-Seed → PVD + CVD Co Liner & Cap → PVD + ALD Barrier → PVD + Selective Barrier & RuCo Liner + Cu Reflow

**CONTACTS = TUNGSTEN → MOLY |** Connecting transistors to interconnects

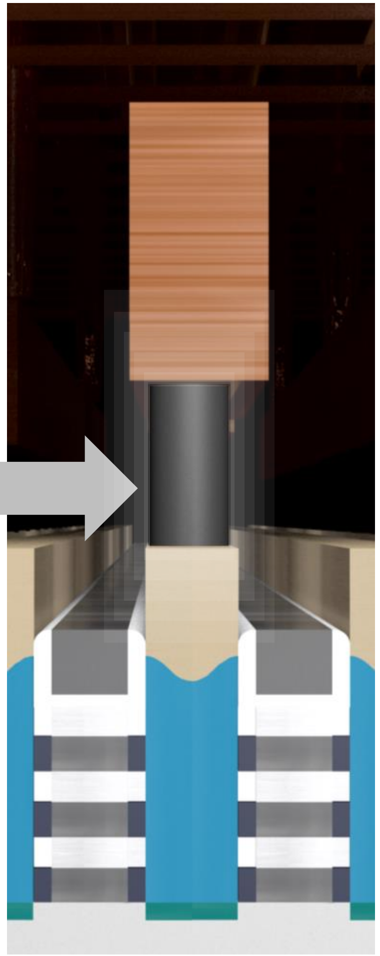
CVD W Fill & TiN Barrier → CVD W Fill & WC Barrier → CVD Co Fill & thin TiN Barrier → Selective CVD W Fill

**TRANSISTORS |** High-speed switching

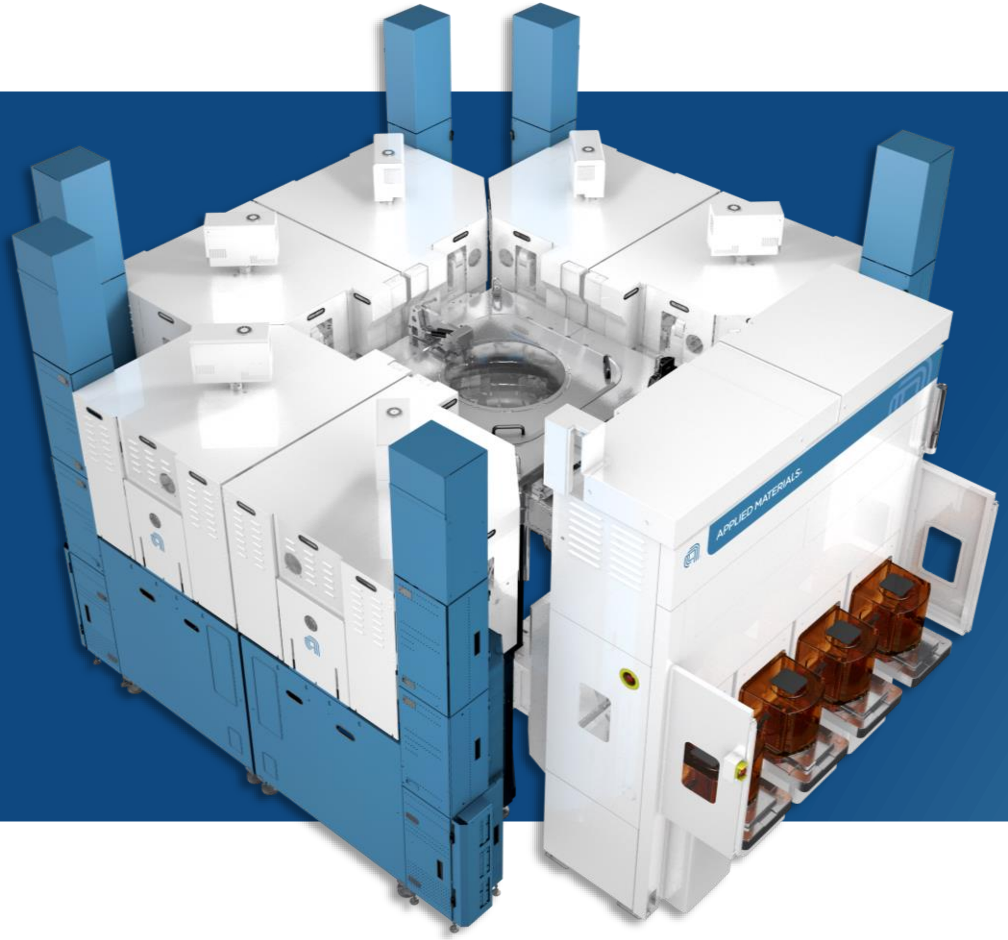
PLANAR → FINFET → GATE-ALL-AROUND

**Nodes** ≥ 20nm 16/14nm ≤ 2nm

New: Selective ALD Mo Fill



# Applied Centris™ Spectral™ Moly ALD

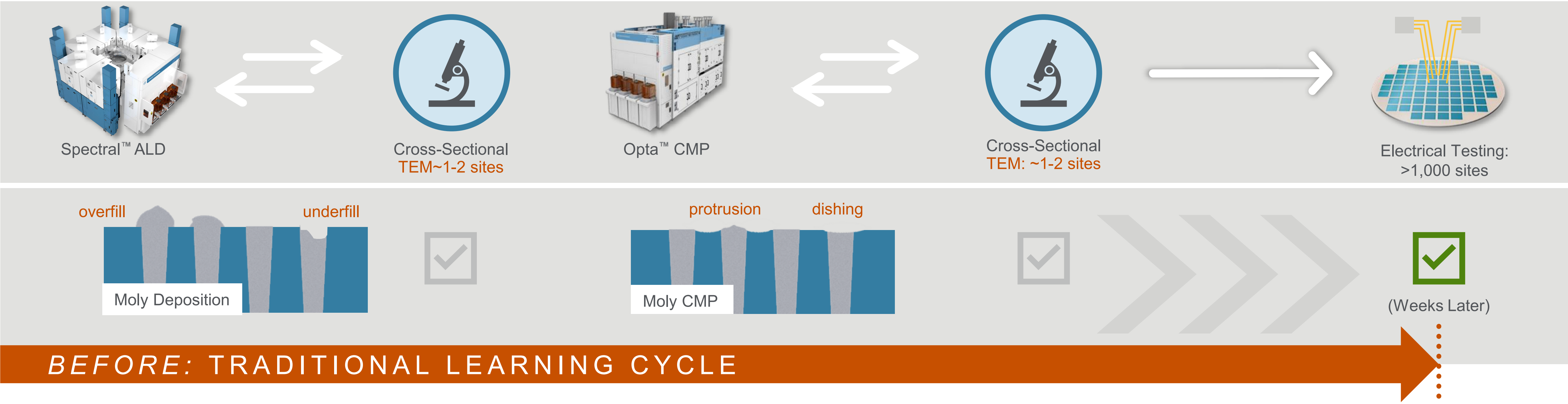


- ✓ State-of-the-art ALD delivers atomic-level control for moly deposition
- ✓ Employs >25 years of expertise in selective materials processing
- ✓ Reduces contact resistance by 15%* vs. selective tungsten in critical vias

*at 12nm via widths using Applied Materials internal test vehicle

## Being adopted by multiple leading-edge F/L customers

# eBeam + AI Tools Accelerate Process R&D: Moly Case Study



Spectral™ ALD

Cross-Sectional
TEM~1-2 sites

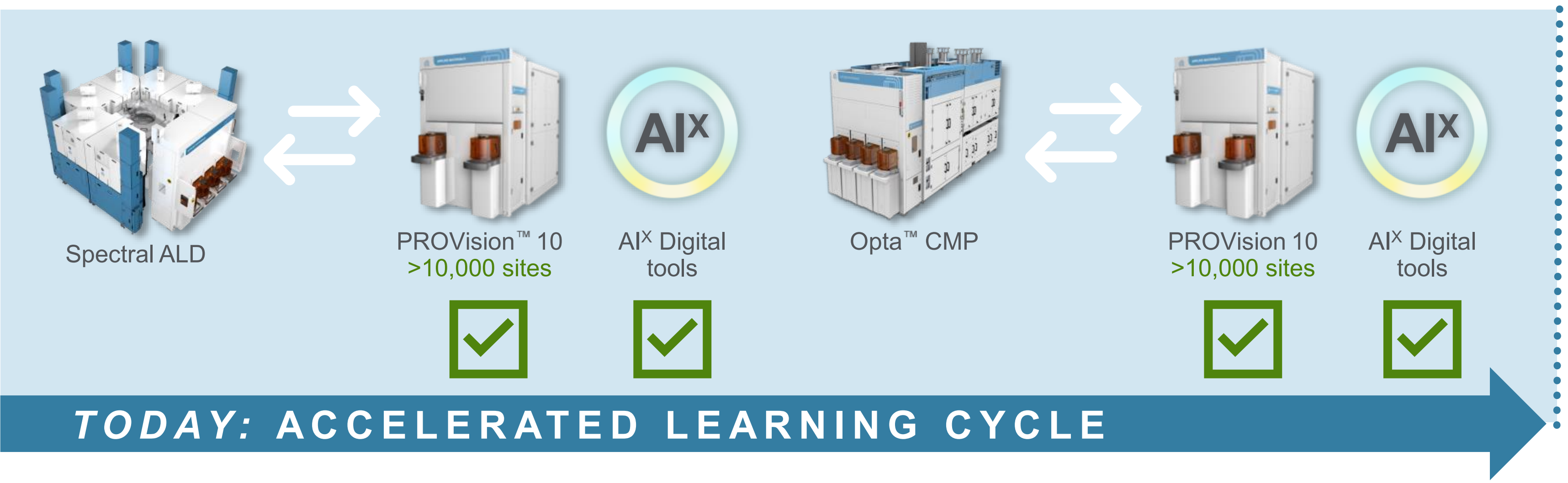
Opta™ CMP

Cross-Sectional
TEM: ~1-2 sites

Electrical Testing:
>1,000 sites

☑
(Weeks Later)

**BEFORE: TRADITIONAL LEARNING CYCLE**



Spectral ALD

PROVision™ 10
>10,000 sites
☑

AI$^{X}$ Digital
tools
☑

Opta™ CMP

PROVision 10
>10,000 sites
☑

AI$^{X}$ Digital
tools
☑

**TODAY: ACCELERATED LEARNING CYCLE**

Close the Loop in
**Hours** versus Weeks

# Inflection-Focused Innovation

**Co-Innovate**
With customers to identify and address most valuable technology solutions with uniquely broad portfolio

**Deliver**
Valuable new products, chip manufacturing processes and AIx services

**Create Value**
As customers ramp more valuable silicon sooner, faster, at higher yield, lower cost

**Share Value**
To increase margins, R&D investments, cash to shareholders

> “At Applied Materials, our strategy is inflection-focused innovation. By focusing our R&D resources on the development of high-value solutions to enable major device architecture inflections, we are accelerating our customers' roadmaps and driving sustainable value capture and margin expansion for Applied. Our innovators have generated an expansive pipeline of next-generation products.
>
> *CEO Earnings Commentary, Feb. 12, 2026*

ANNOUNCED

# **Samsung Electronics**
## **joins EPIC Center**

Co-development programs to accelerate commercialization of next-generation semiconductor technologies

# Calendar Announcements

**APRIL 8 | 9AM PT**

Transistors and Wiring Master Class

Webcast

**2H FY2026**

Additional Master Classes

Webcasts

**OCTOBER 12**

Investor Open House at the New EPIC Center in Silicon Valley

Sunnyvale, CA

**OCTOBER 13**

Investor Breakfast at SEMICON West

San Francisco, CA | Webcast

APPLIED
MATERIALS™

Material Innovation