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NEWS RELEASE

Applied Materials Technologies Enable 2D Scaling with EUV and 3D Gate-All-Around Transistors

- *Applied extends 2D EUV logic scaling with Stensar™ CVD alternative to spin-on patterning films*
- *Previews broadest portfolio of technologies for 3D Gate-All-Around transistors including two new Integrated Materials Solutions™*

SANTA CLARA, Calif., April 21, 2022 – Applied Materials, Inc. today introduced innovations that help customers continue 2D scaling with EUV and detailed the industry's broadest portfolio of technologies for manufacturing next-generation 3D Gate-All-Around transistors.

Chipmakers are pursuing two complementary paths to increase transistor density in the years ahead. One is classic Moore's Law 2D scaling, creating smaller features using EUV lithography and materials engineering. The other is using design technology cooptimization (DTCO) and 3D techniques that cleverly optimize the layout of logic cells to increase density independent of changes in the lithography pitch. These latter approaches, which include backside power distribution networks and Gate-All-Around (GAA) transistors, are expected to drive a growing proportion of logic density improvements in future years as classic 2D scaling slows. Together, these techniques can help chipmakers as they aim to deliver future generations of logic chips with improved power, performance, area, cost and time-to-market – or PPACt.

"Applied's strategy is to be the PPACt enablement company™ for our customers, and today we are presenting seven innovations designed to enable customers to continue 2D scaling with EUV," said Dr. Prabu Raja, Senior Vice President and General Manager of the Semiconductor Products Group at Applied Materials. "We are also detailing how GAA transistors will be manufactured in fundamentally different ways than today's FinFET transistors, and how Applied is ready with the broadest product line for GAA manufacturing including new steps in epitaxy, atomic layer deposition and selective materials removal along with two new Integrated Materials Solutions™ for creating ideal GAA gate oxides and metal gates."

Extending 2D Scaling

The emergence of extreme ultraviolet (EUV) lithography has enabled chipmakers to produce smaller features and increase transistor density. However, the industry has reached a point where further scaling with EUV is introducing challenges that require new approaches to deposition, etch and metrology.

Following EUV resist development, chip patterns need to be etched through a series of intermediate layers – called the transfer layer and hardmask – before they are finally etched into the wafer. Until now, these layers have been deposited using spin-on technology. Today, Applied is introducing the Stensar™ Advanced Patterning Film for EUV which is deposited using Applied's Precision CVD (chemical vapor deposition) system. Compared to spin-on deposition, Applied's CVD film helps customers tune the EUV hardmask layers for specific thicknesses and etch resiliency so they can achieve near-perfect EUV pattern transfer uniformity across the entire wafer.

Applied also detailed a special capability of its Sym3® Y etch systems which enables customers to etch and deposit materials in the same chambers to help improve EUV patterns before they are etched into the wafer. The Sym3 chambers gently remove EUV resist materials and then redeposit material in a special way that averages out the pattern variability caused by "stochastic errors." The improved EUV patterns increase yields and improve chip power and performance. As a result, Applied's Sym3 technology is quickly growing beyond memory – where Applied is the number-one supplier of conductor etch systems to the DRAM market – to foundry-logic.

Applied also demonstrated how its PROVision® eBeam metrology technology can be used to see deeply within multilayer chips to precisely measure EUV-patterned features across the entire wafer, helping customers solve "edge placement errors" that other metrology techniques cannot diagnose. Applied nearly doubled its eBeam system revenue in 2021 and has become the number-one supplier of eBeam technology.

Engineering 3D Gate-All-Around Transistors

The emerging GAA transistor exemplifies how customers can supplement 2D scaling with 3D design techniques and DTCO layout innovations to rapidly increase logic density even as 2D scaling slows. Innovations in materials engineering provide GAA transistors with improvements in power and performance as well.

In FinFETs, the vertical channels that form the transistor's electrical path are determined by lithography and etch, processes that result in uneven channel widths. The non-uniformity negatively impacts power and performance, which is one of the major reasons customers are moving to GAA.

GAA transistors resemble FinFET transistors that have been rotated by 90 degrees so that the channels are horizontal instead of vertical. The GAA channels are formed using epitaxy and selective materials removal, technologies that enable customers to precisely engineer the width and uniformity for optimum power and performance. Applied's first-ever product was an epitaxy system, and the company has been the market leader ever since. Applied pioneered selective materials removal when it launched the Selectra® system in 2016 and is the market leader with over 1,000 chambers in use by customers.

A major challenge of manufacturing GAA transistors is that the space between the channels is only around 10nm, and customers must deposit the multilayer gate oxide and metal gate stacks around all four sides of the channels in the minute space available.

Applied has developed an IMS™ (Integrated Materials Solution) system for the gate oxide stack. A thinner gate oxide results in higher drive current and transistor performance. However, thinner gate oxides typically result in higher leakage current that wastes power and creates heat. Applied's new IMS system reduces equivalent oxide thickness by 1.5 angstroms, enabling designers to increase performance with no increase in gate leakage or keep performance constant and reduce gate leakage by more than 10X. It integrates atomic layer deposition (ALD), thermal steps, plasma treatment steps and metrology in a single, high-vacuum system.

Applied is also demonstrating an IMS system for engineering GAA metal gate stacks, enabling customers to vary gate thicknesses in order to tune transistor threshold voltages to meet the performance-per-watt goals of specific computing applications ranging from battery-powered mobile devices to high-performance servers. It performs the high-precision metal ALD steps in high vacuum to prevent atmospheric contamination.

Additional details about Applied's logic scaling solutions will be provided at the company's "New Ways to Shrink" Master Class being held later today.

About Applied Materials
Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible a better future. Learn more at www.appliedmaterials.com.

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