Wafer Fab Equipment
MARKET BRIEFING

MAY 2, 2024

APPLIED MATERIALS®
make possible

Forward-Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and market share positions, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products, our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; global economic, political and industry conditions, including rising inflation and interest rates; the implementation and interpretation of new export regulations and license requirements, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies; our ability to obtain licenses or authorizations on a timely basis, if at all; consumer demand for electronic products; the demand for semiconductors; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the effects of geopolitical turmoil or conflicts, and of regional or global health epidemics; our ability to accurately forecast market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

https://ir.appliedmaterials.com/events

AGENDA

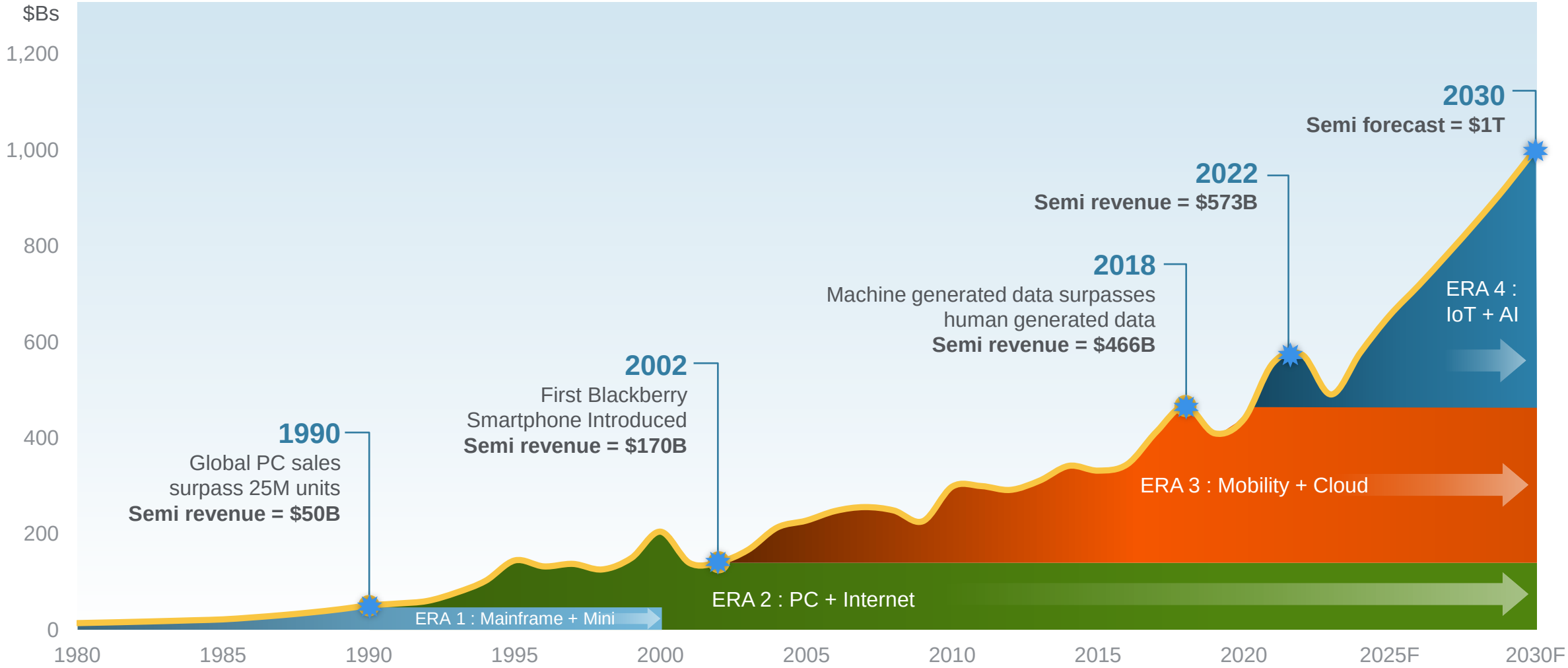
WFE Market History and Evolution

2023 WFE Market

Applied Materials Markets and Position

Applied Materials Growth Thesis

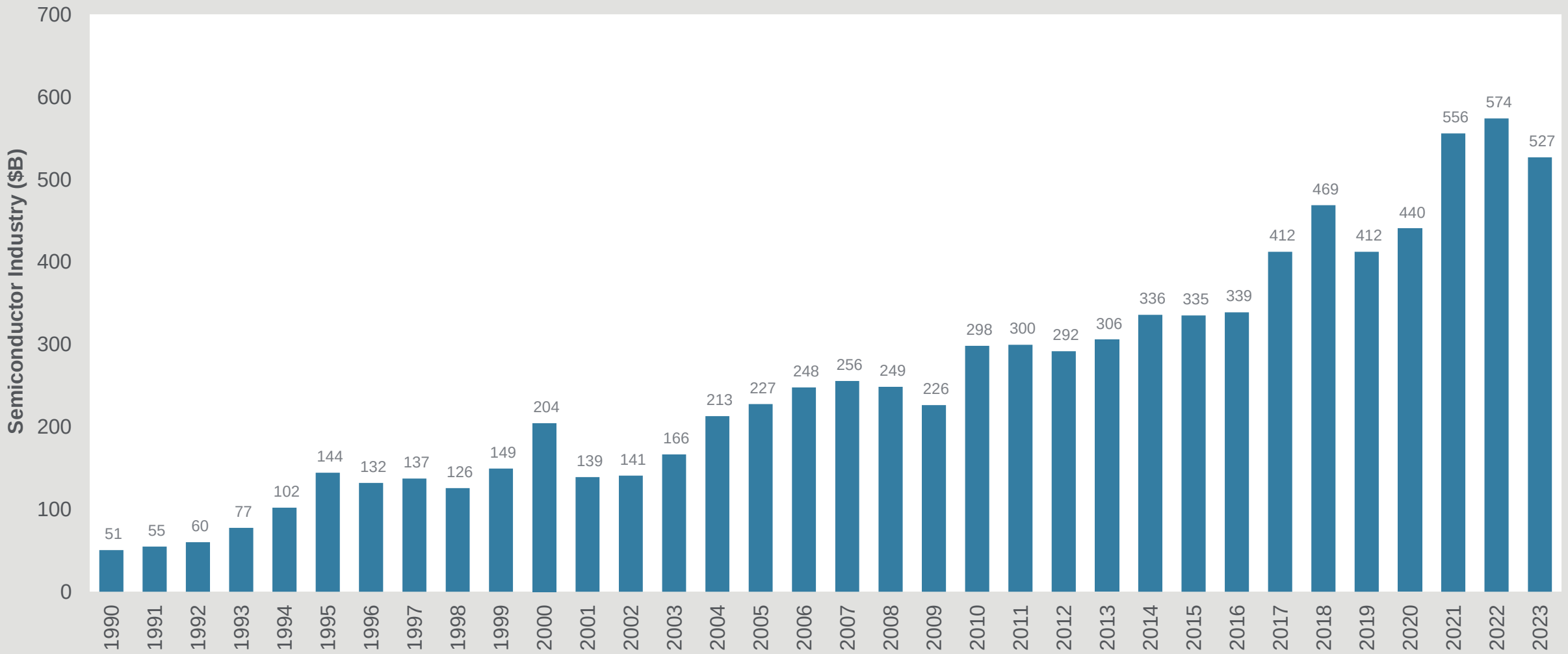
Our Semiconductor Industry Market Thesis



IoT + AI Era is the 4th and Biggest Age of Computing

Source 2030 forecast: TechInsights, McKinsey & Company, SEMI. Source Historical data: SIA, TechInsights, Applied Materials.

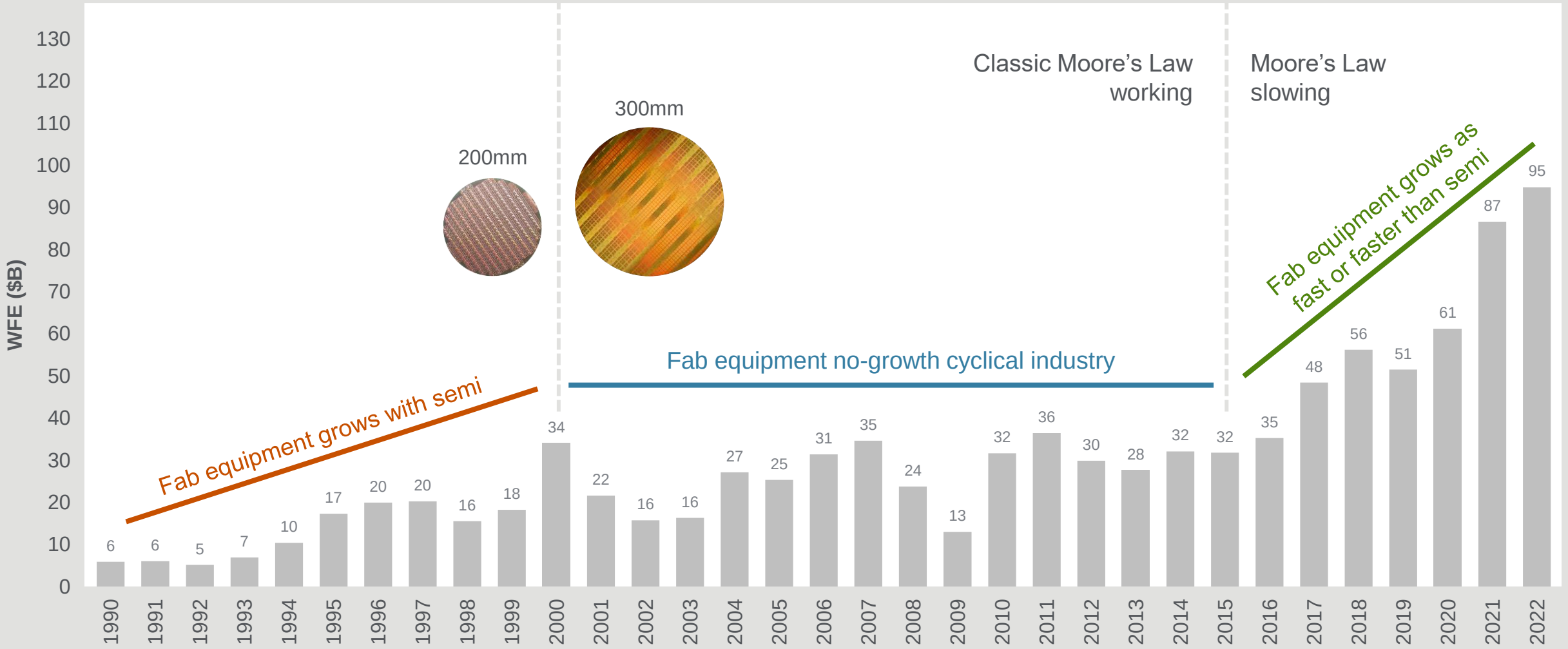
Semiconductor Revenue



Source: SIA, TechInsights

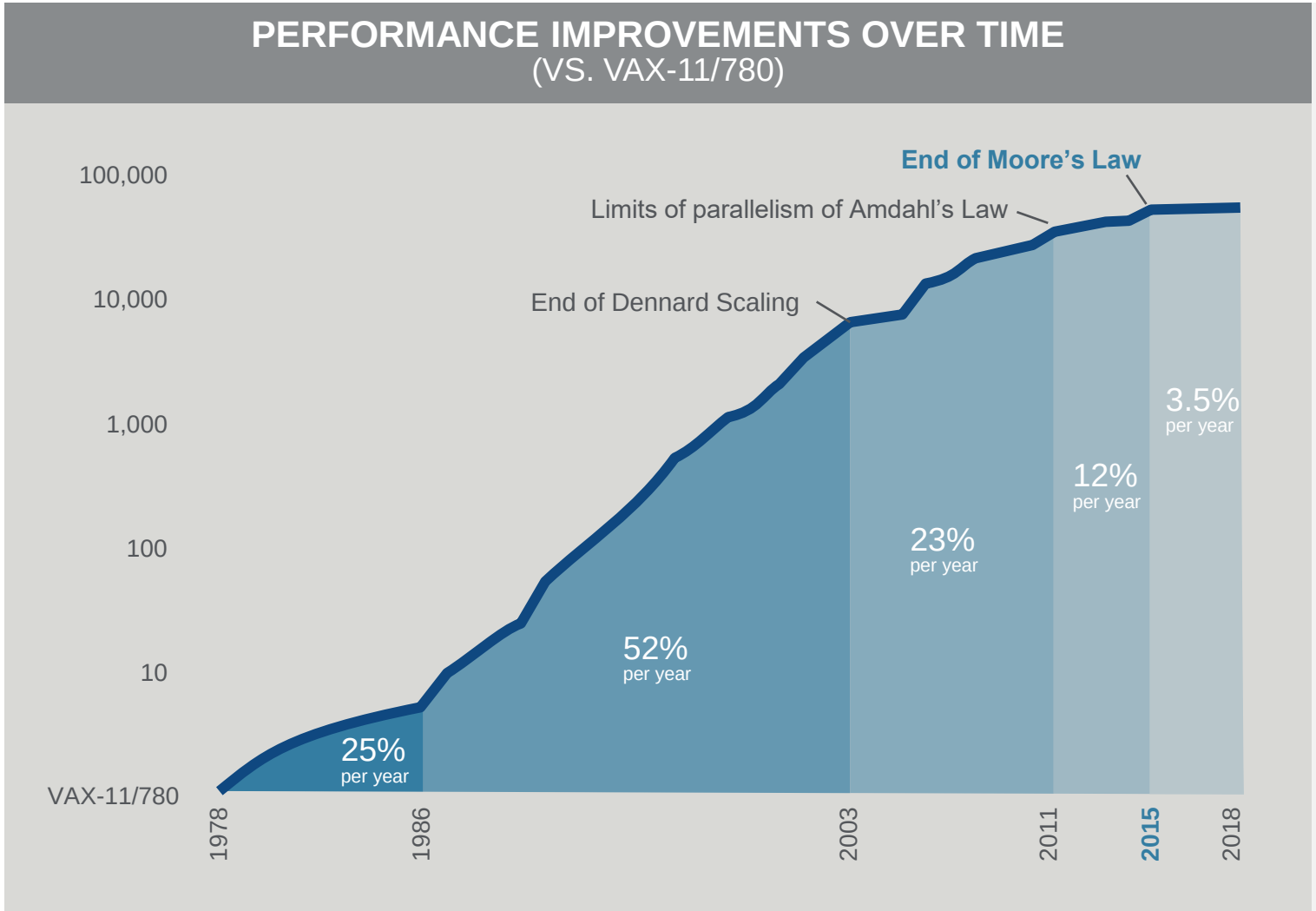
APPLIED MATERIALS

Wafer Fab Equipment Spending



Source: Gartner, TechInsights, Applied estimates

2015: Classic Moore's Law Slows

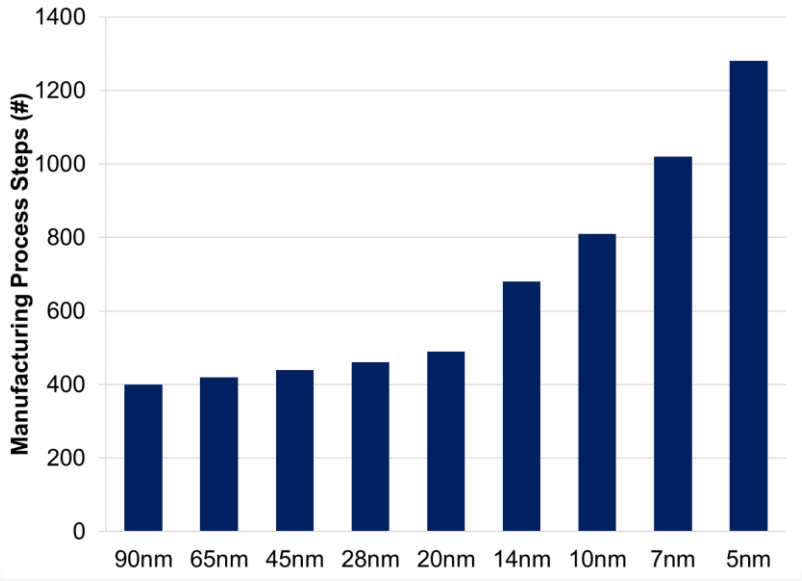


For most of the industry's history, the number of transistors on a microprocessor doubled about every two years and drove simultaneous improvements in performance, power and cost.

Today, transistors are shrinking at a slower rate; **improving performance and power requires new processor architectures, transistor architectures and materials engineering techniques;** and cost is increasing.

Source: Computer Architecture: A Quantitative Approach, Sixth Edition, John Hennessy and David Patterson, December 2017

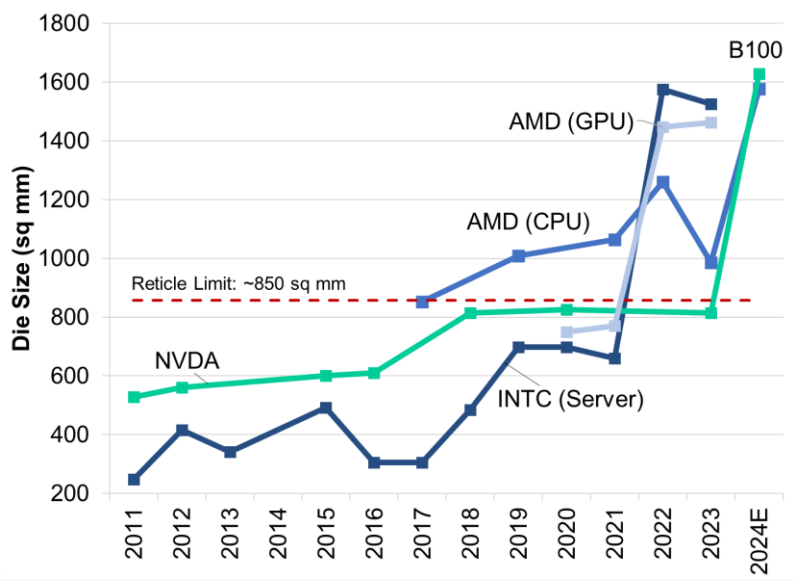
Semiconductor Complexity and Die Sizes Increasing



Process Steps

90nm→20nm: process steps increase by ~5% per node

20nm→5nm: process steps increase by ~28% per node



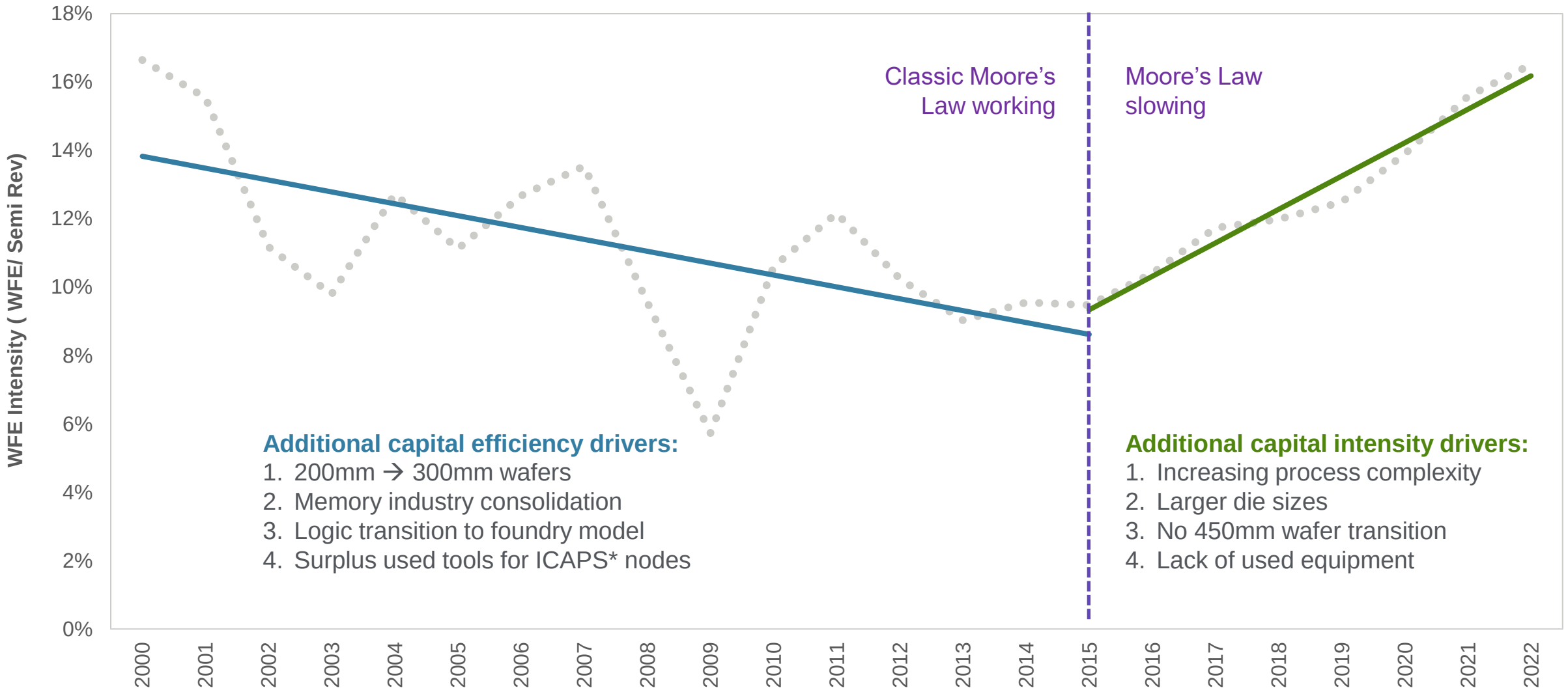
Server Die Sizes

AI datacenter processors now use chiplet architecture which allows chips to scale beyond the reticle limit

Data center processor die sizes have increased by as much as 5X

Source: Evercore ISI Research; (1) Evercore ISI Research, electriiq.com, Applied Materials presentation; (2) company data, Evercore ISI Research, Anandtech, wccftech.com, techpowerup.com, Locuza

WFE Intensity Inflection



Source: SIA, SMI, Applied Materials
*ICAPS = Internet of Things, Communications, Automotive, Power, Sensors; includes F/L spending at 10nm and above nodes.

AGENDA

WFE Market History and Evolution

2023 WFE Market

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Applied Materials Growth Thesis

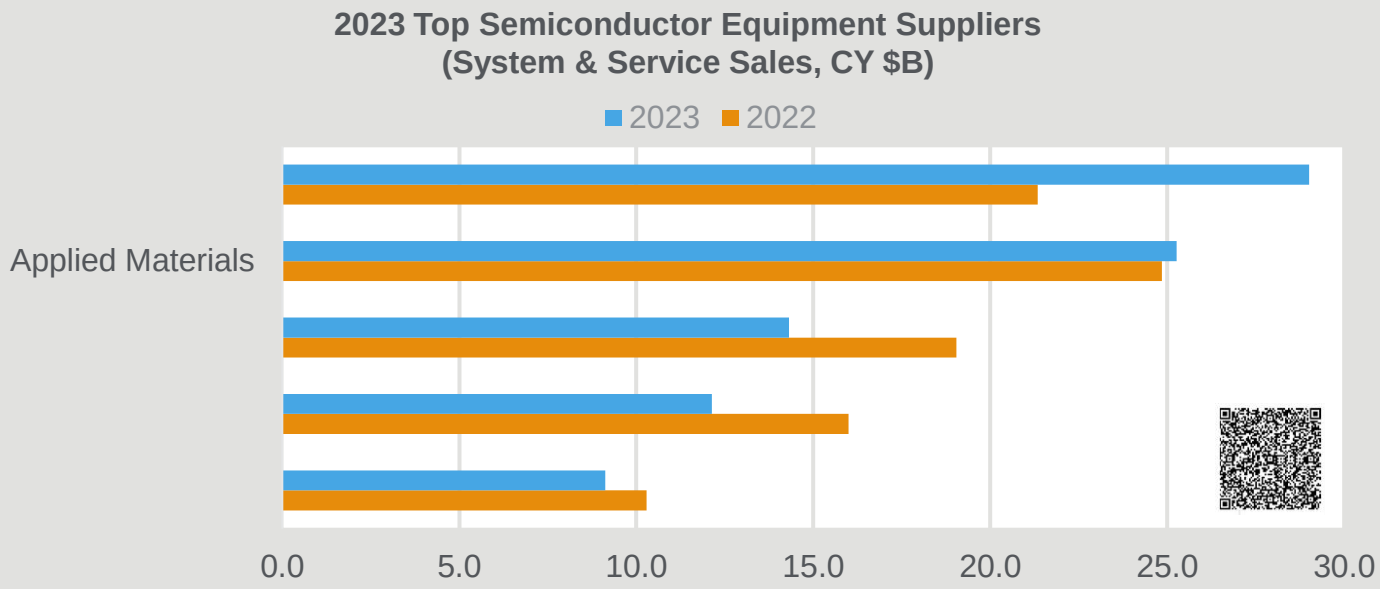
Tech Insights Wafer Fab Equipment Market Report

2023 Top Equipment Suppliers

April 9, 2024

Lyndsey Lindt
Senior Market Research Analyst

Nhi Than
Market Research Analyst

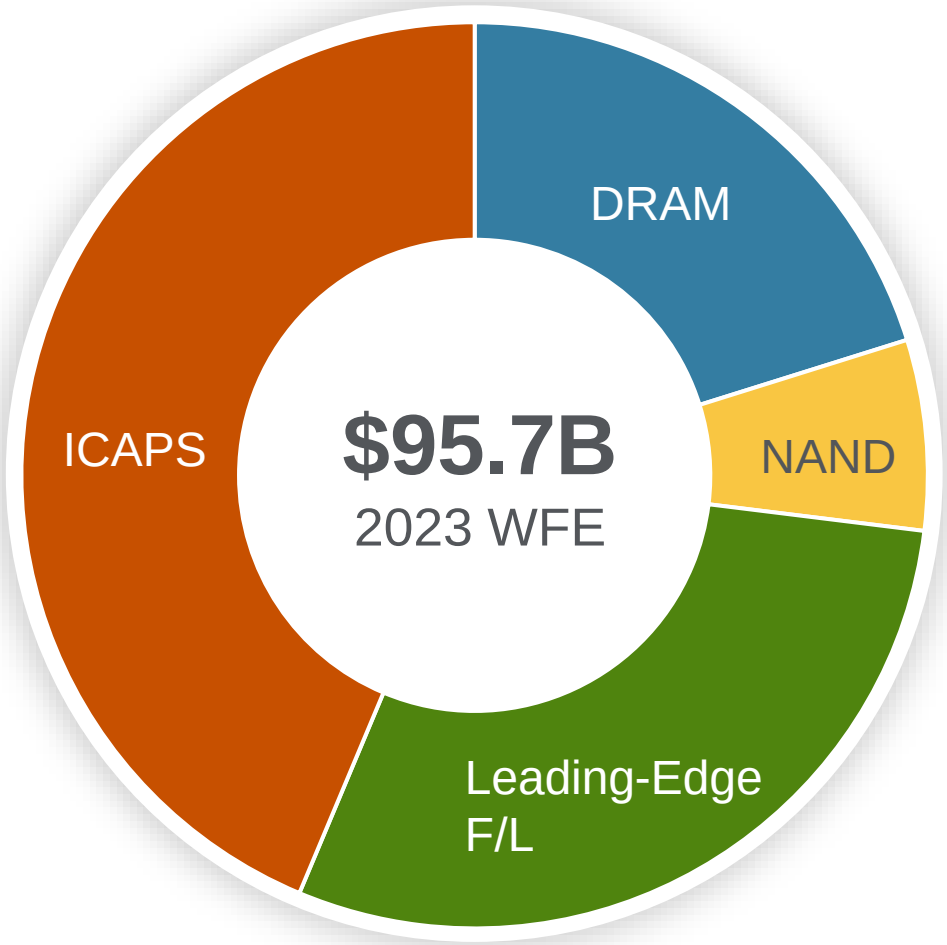


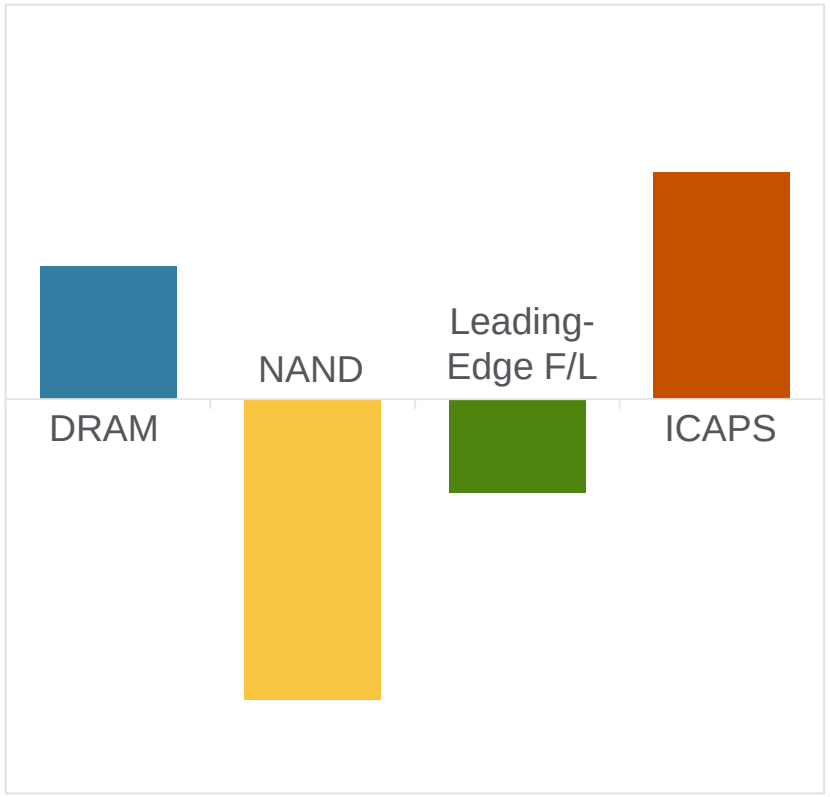
2023 WFE: $95.7B, +1%, ~3X 2015 WFE

Source: TechInsights, released April 2024. Wafer Fabrication Equipment (WFE) = front end equipment and excludes "other WFE" of $2.9B.

APPLIED MATERIALS

2023 WFE by Device





Advanced Packaging WFE:
~$3.9B (+18% YoY)
Included within device WFE

Source: TechInsights, Applied Materials analysis.
ICAPS = Internet of Things, Communications, Automotive, Power, Sensors; includes F/L spending at 10nm and above nodes.
Advanced packaging includes front-end WFE sales for packaging applications

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Applied Materials Technologies

Materials Engineering

Create and deposit


Epitaxy


Metal deposition


Dielectric deposition


Plating


ALD


Selective deposition

Shape and remove


Etch

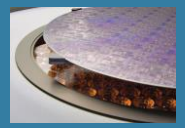

Planarization


Selective removal


Pattern shaping

Modify


Implant


Thermal


Treatments

Process Control

Analyze


Optical inspection

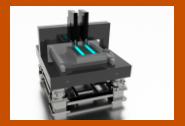

Defect review


eBeam metrology and inspection

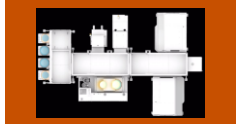

CD-SEM

Connect

Heterogeneous Integration


Digital lithography

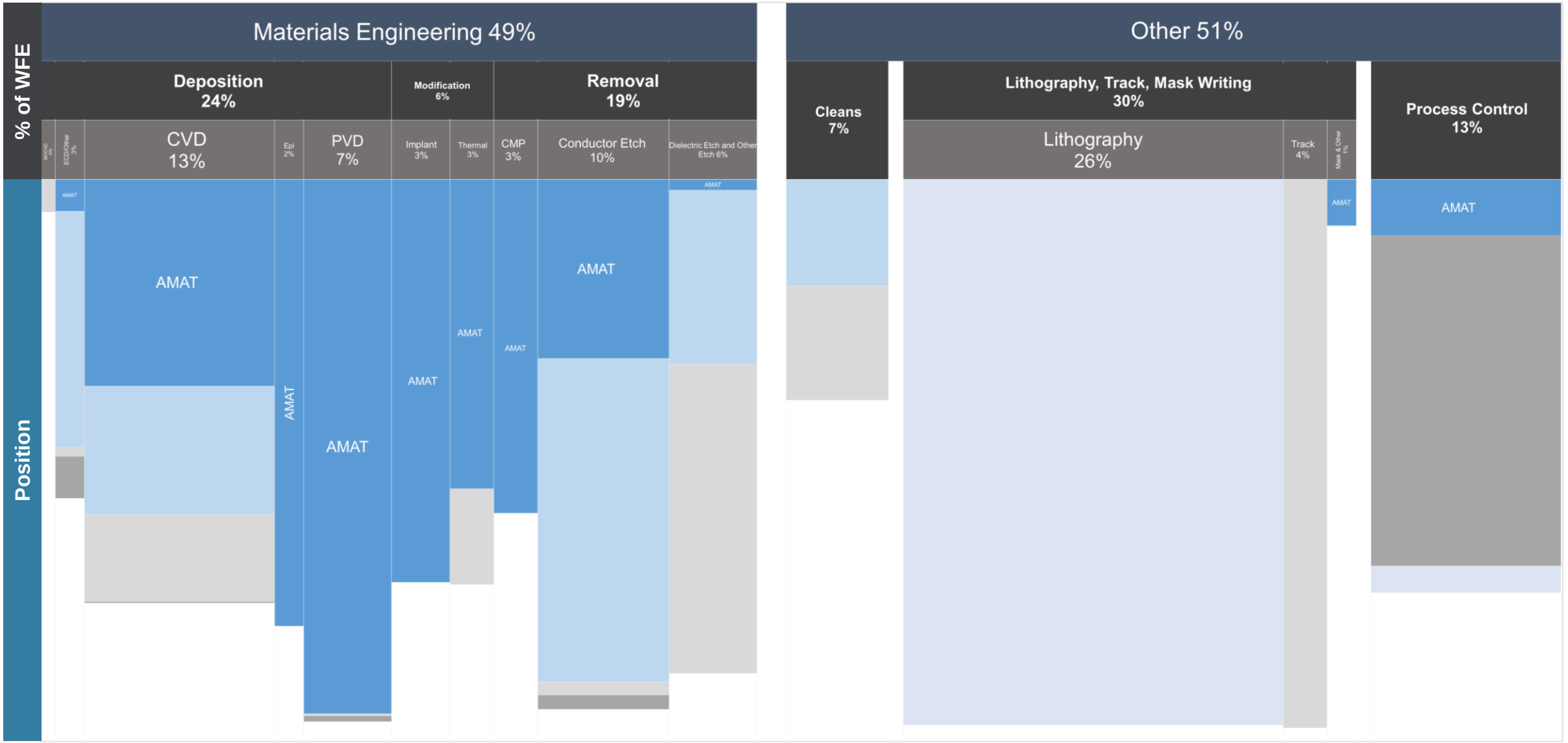

Panel-level PVD


Hybrid bonding


eBeam Test

Learn more: "How do you make a chip" video

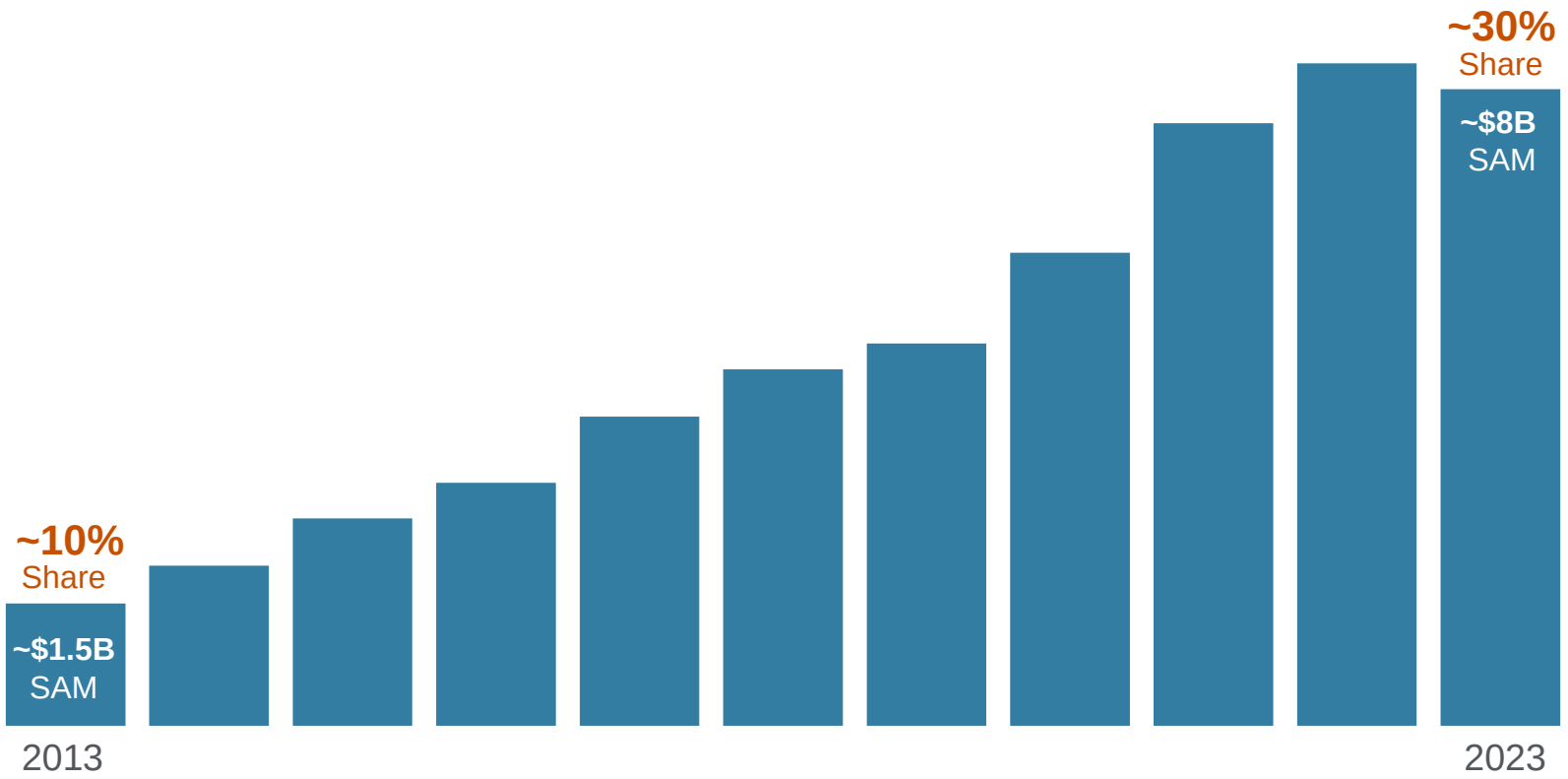
2023 WFE ($95.7B) by Technology



Source: TechInsights, released April 2024. Wafer Fabrication Equipment (WFE) = front end WFE and excludes “other WFE” of $2.9B. CVD includes ALD

APPLIED MATERIALS

Applied Materials Patterning Served Markets and Share



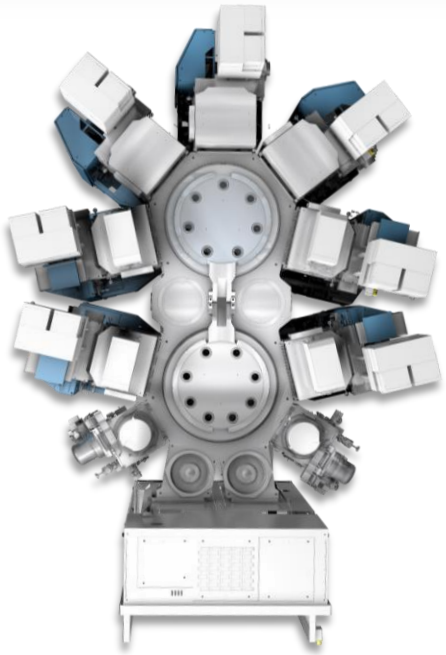
* Patterning SAM and share includes Foundry/Logic and DRAM, excludes NAND

Industry's Broadest Portfolio
ALD
CMP
CVD
Etch
Metrology
Pattern Shaping
Selective Materials Removal
Thermal

Applied's Patterning Revenue has Grown at ~2.5X the Rate of WFE

Source: Applied Materials analysis

How We Deliver Materials Engineering Technologies



Endura PVD

Unit Processes

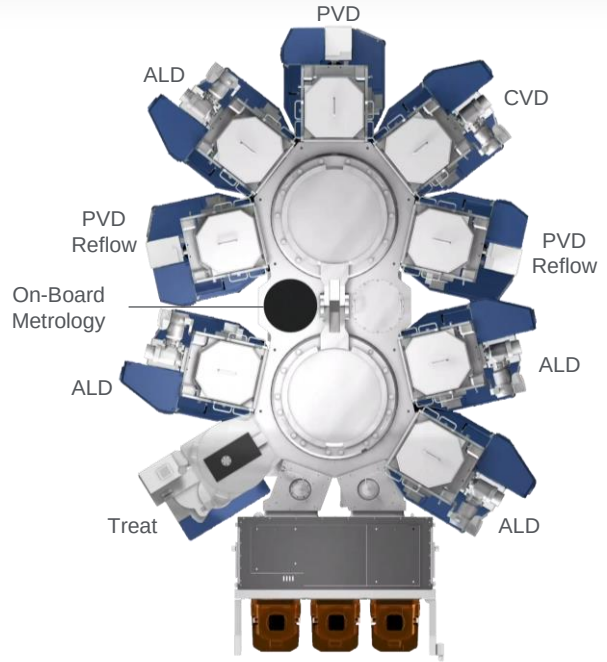
One technology in one system

Producer CVD

Centris Sym3 Etch

Co-optimized Processes

Two or more co-optimized technologies in adjacent systems



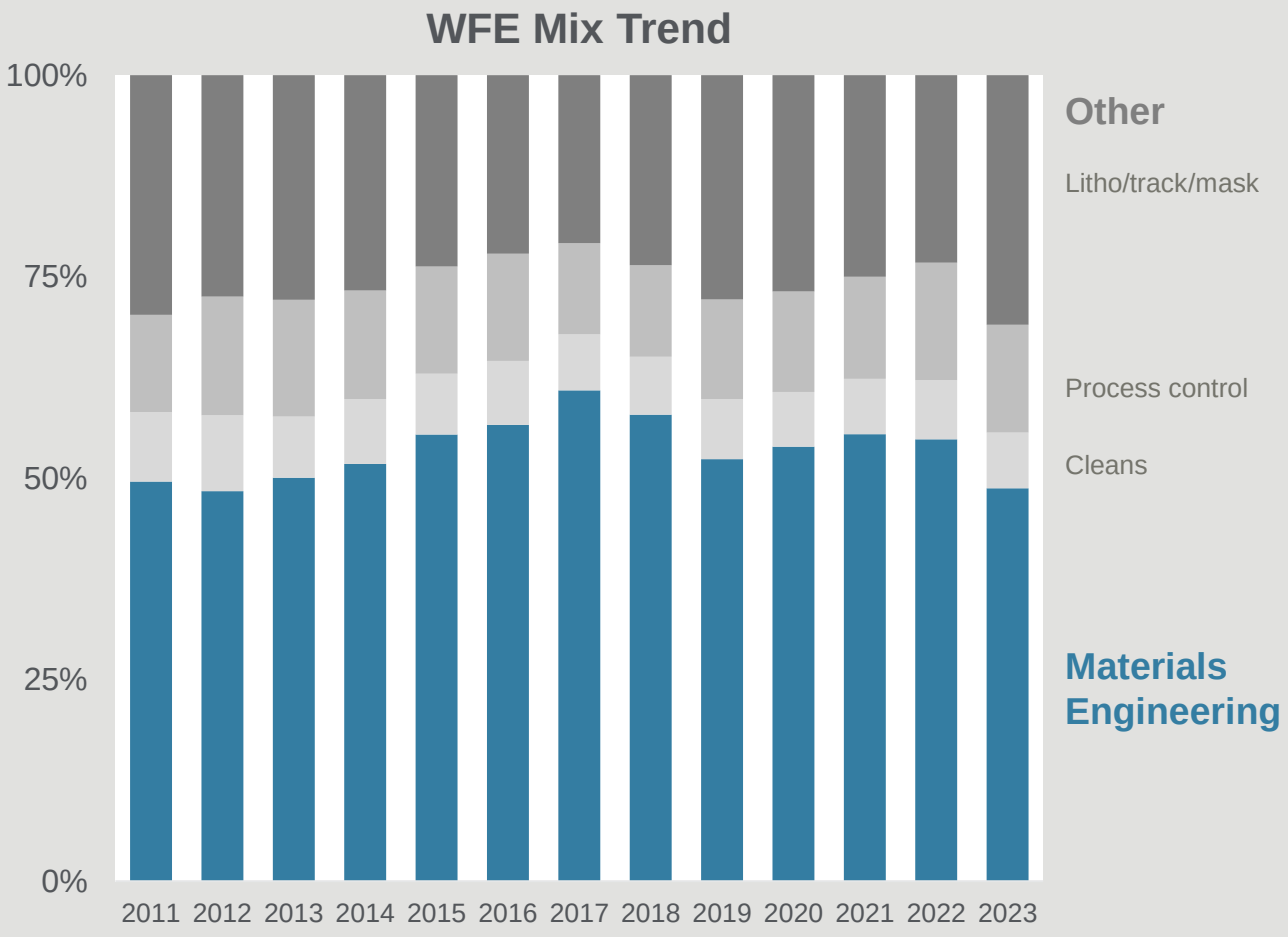
Example: Endura IMS™ (Integrated Materials Solution)

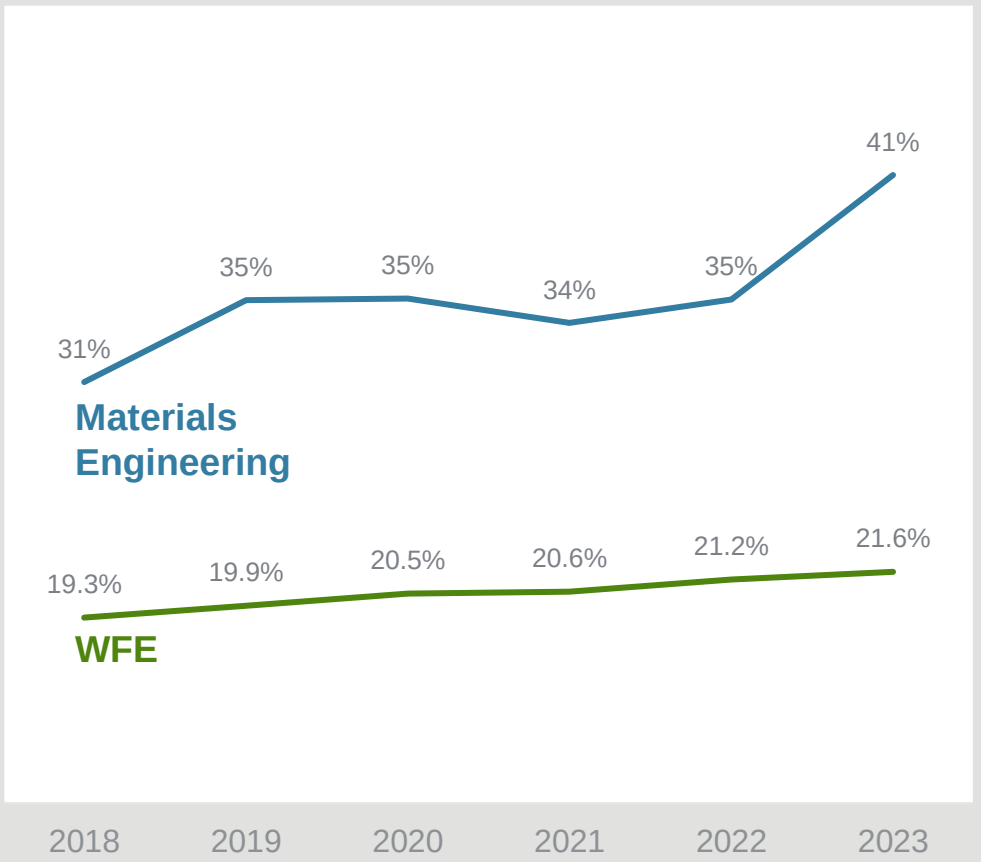
Integrated Processes

Two or more co-optimized technologies in one system

IMS Represented ~30% of Semi Systems Revenue in FY23 (vs ~20% in FY19)

WFE Market Trends





Applied Gained WFE Share in Each of Past 5 Years and is #1 in Materials Engineering

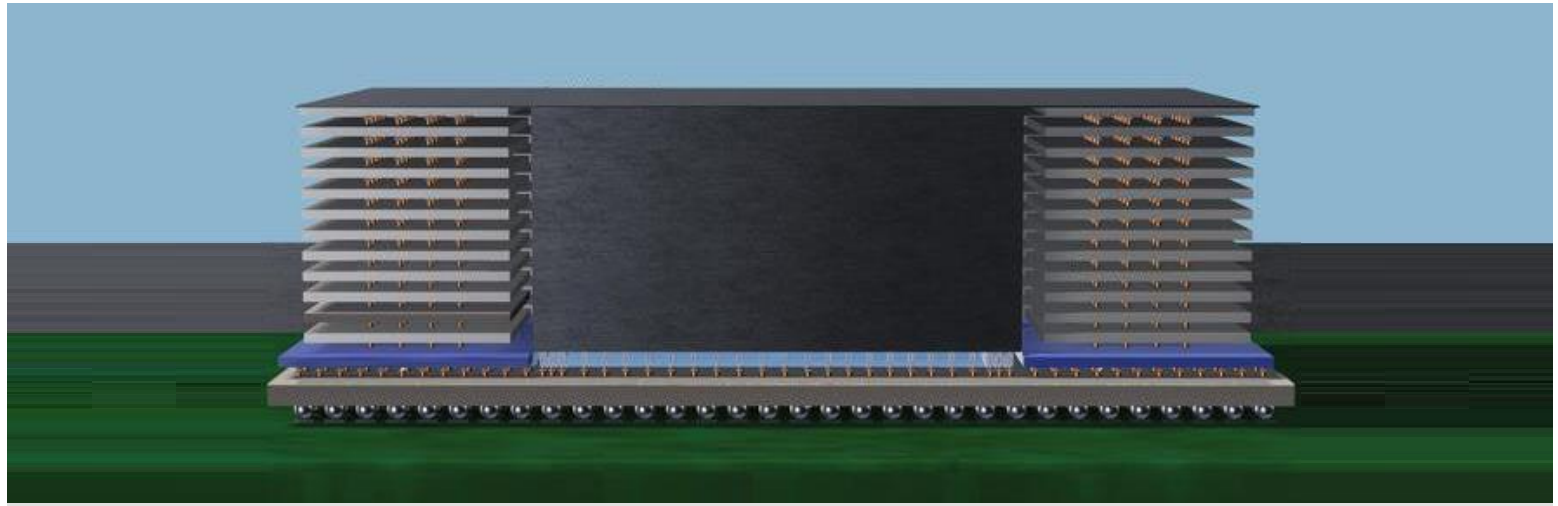
Source: Gartner (2011-19), TechInsights (2020-23), Applied Materials analysis. Materials Engineering is creating and depositing materials; shaping and removing materials; modifying materials; and connecting chips with advanced packaging. The related equipment categories are deposition (MOCVD, ECD/other, CVD, Epi PVD), modification (Implant, Thermal) and removal (CMP, etch). Materials Engineering excludes litho/track/mask, process control and cleans.

2023 Applied Materials WFE Share by Device

Device	WFE Share
Leading-edge F/L	~21%
ICAPS	~23%
DRAM	~23%
NAND	<15%

Advanced packaging:

~30% WFE share
~50% SAM share
~50% SAM share of HBM



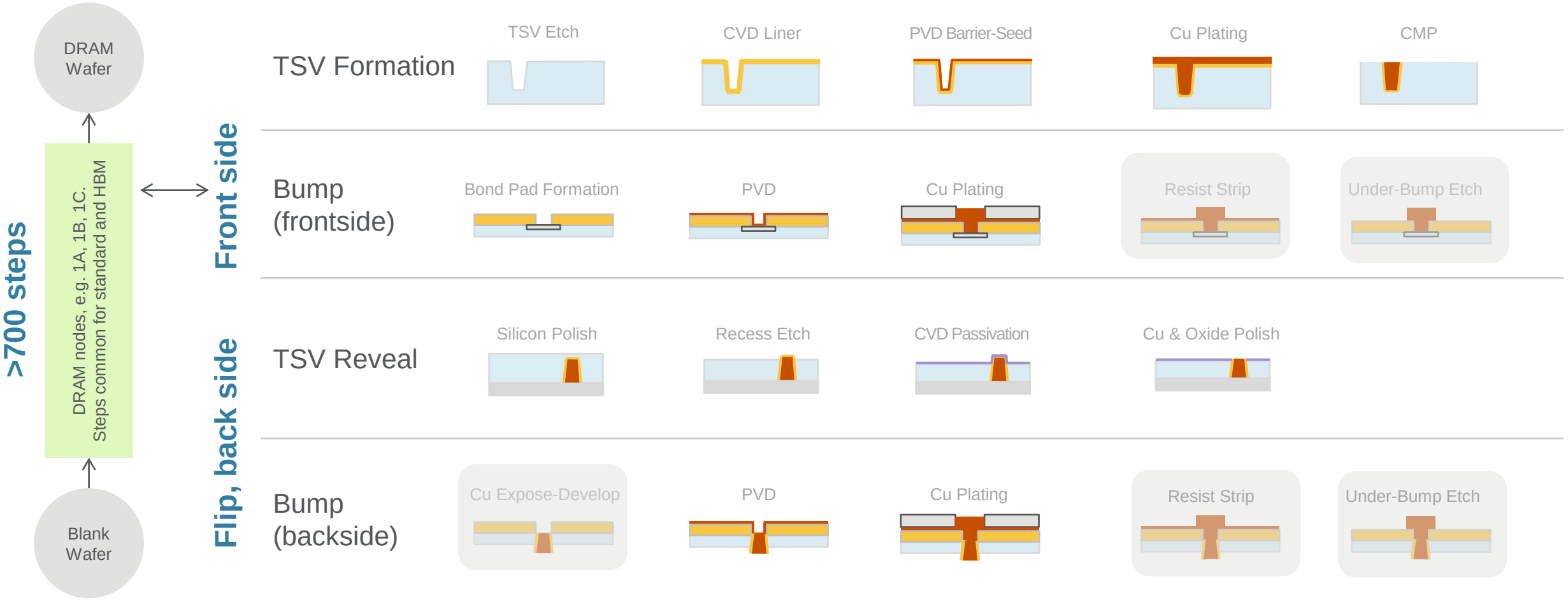
DRAM Leadership

increased share by 10pts in 10 years

- » Ported transistor integrated materials solutions from logic to DRAM to increase DRAM I/O speed
- » Gained share in DRAM patterning with co-optimized Draco® CVD and Sym3® etch for capacitor scaling
- » Largest supplier of advanced packaging solutions, enabling multiple generations of HBM

Source: TechInsights, Applied Materials analysis. ICAPS = IoT, Communications, Automotive, Power, Sensors; includes F/L spending at 10nm and above nodes.
Advanced packaging includes front-end WFE sales for packaging applications. Packaging/HBM SAM includes CVD, PVD, etch, CMP, plating

High-Bandwidth Memory: Incremental Materials Engineering Steps



- Applied's broad portfolio supports ~3/4 of HBM materials engineering process steps
- #1 in HBM with SAM share ~50%

Source: Applied Materials analysis

AGENDA

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2023 WFE Market

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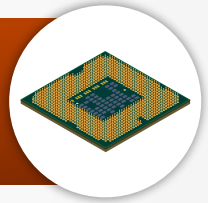
Applied Materials Growth Thesis

Growth Thesis

Global GDP

Semiconductors



Wafer Fab Equipment

Applied Semi Systems

Applied Global Services

1. **Semiconductors** significantly outgrow GDP
2. **Fab equipment** grows as fast or faster than semiconductors
3. **Applied Semi Systems** outgrows fab equipment market
4. **Applied Global Services** grows as fast or faster than Semi Systems

Our Strategy

- Deploy our unique materials engineering breadth and depth to be the most enabling technology partner to our customers
- Anticipate key roadmap inflections and deliver enabling solutions critical to competitive advantage in fast-growing markets

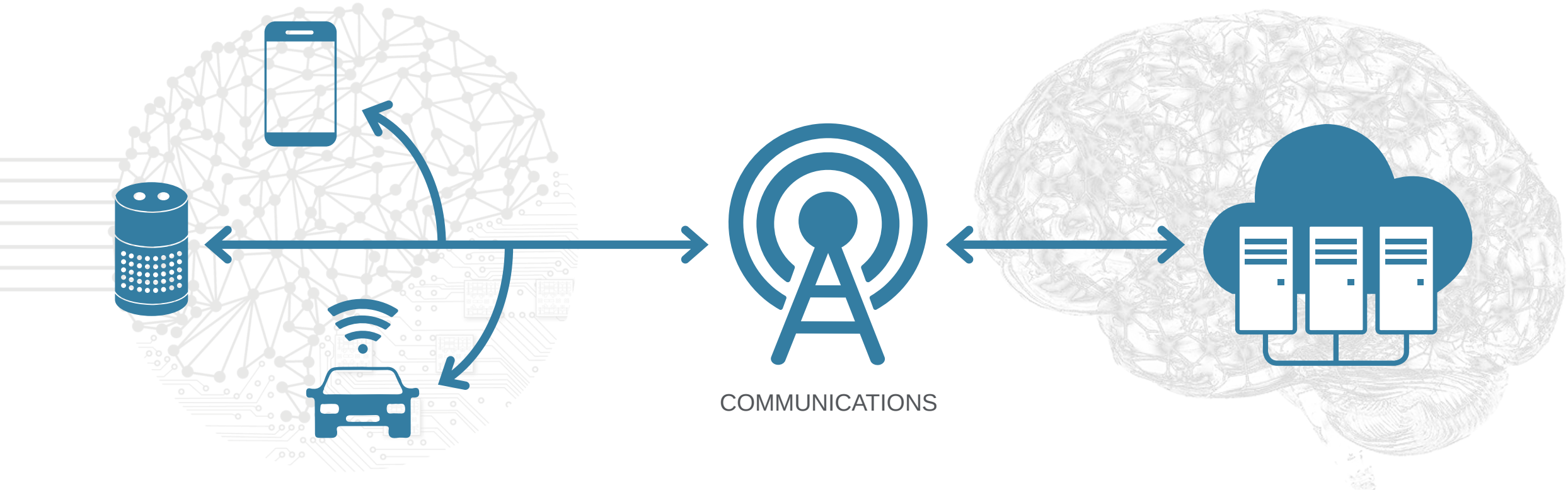
Maydan Technology Center, Sunnyvale CA


META Center, Albany NY

EPIC Center (Planned), Sunnyvale CA


Advanced Packaging Dev. Center, Singapore

AI and WFE



Edge AI/IoT
Drives ICAPS

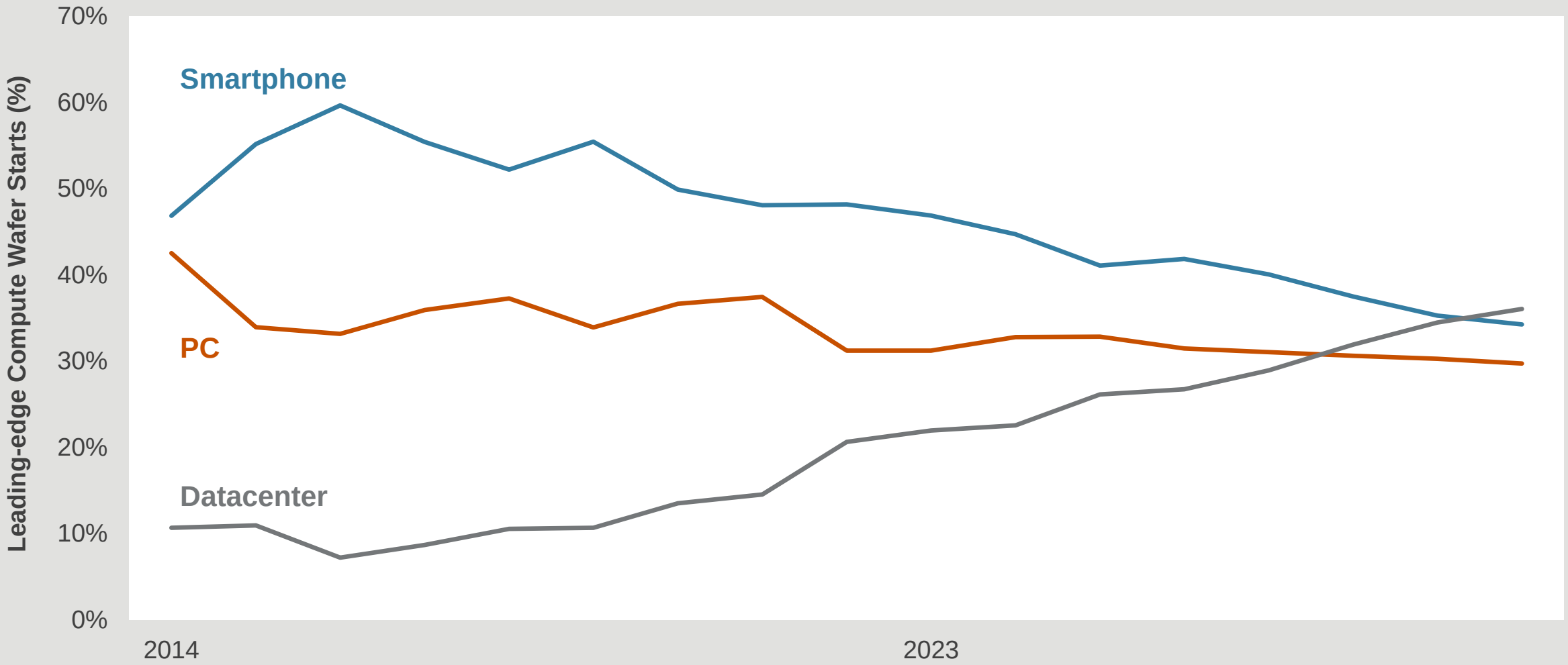
~20% of total WFE in 2023
~20% expected CAGR

Data Center AI
Drives L/E F/L + DRAM

~5% of total WFE in 2023
~30% expected CAGR

Source: Applied Materials analysis. ICAPS = IoT, communications, automotive, power and sensors. Non-AI device segments include non-AI servers, smartphones, PCs, telecommunications equipment and televisions

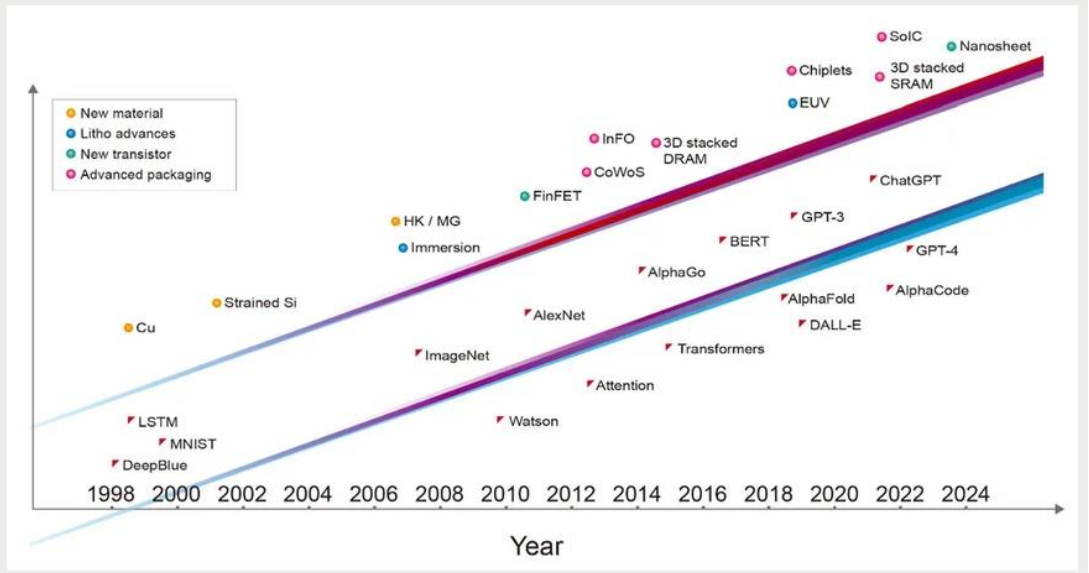
End Market Inflections



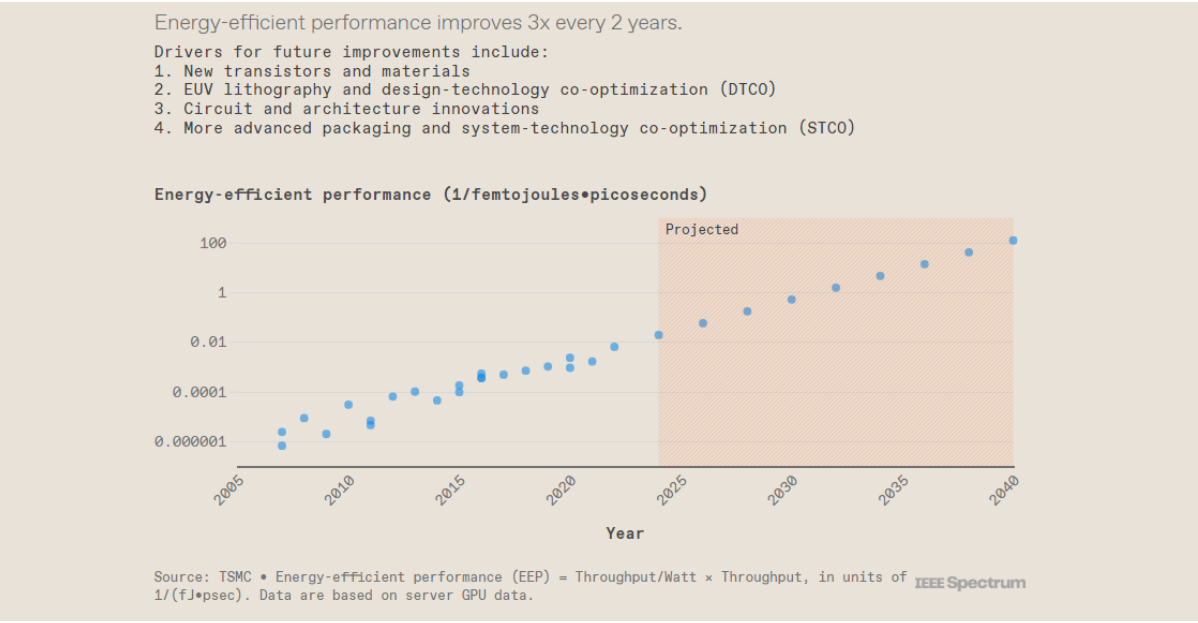
Source: Applied Materials analysis

AI Requirements: More Transistors and Better Energy Efficiency

IEEE Spectrum How We'll Reach a 1 Trillion Transistor GPU



Advances in semiconductor technology [top line]—including new materials, advances in lithography, new types of transistors, and advanced packaging—have driven the development of more capable AI systems [bottom line]



Largely thanks to advances in semiconductor technology, a measure called energy-efficient performance is on track to triple every two years (EEP units are 1/femtojoule-picoseconds).

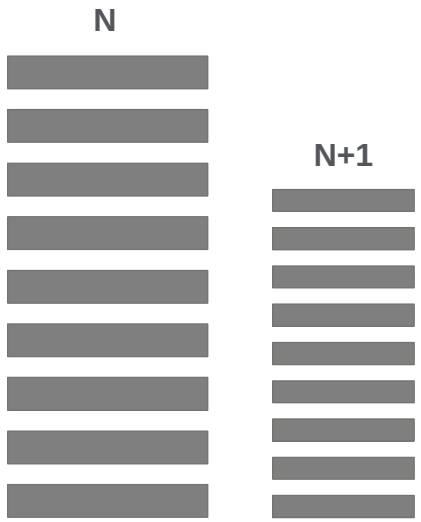
"If the AI revolution is to continue at its current pace, it's going to need even more from the semiconductor industry. Within a decade, it will need a 1-trillion-transistor GPU—that is, a GPU with 10 times as many devices as is typical today."

"For the past 50 years, semiconductor-technology development has felt like walking inside a tunnel. The road ahead was clear, as there was a well-defined path. And everyone knew what needed to be done: shrink the transistor. Now, we have reached the end of the tunnel. From here, semiconductor technology will get harder to develop. Yet, beyond the tunnel, many more possibilities lie ahead. We are no longer bound by the confines of the past."

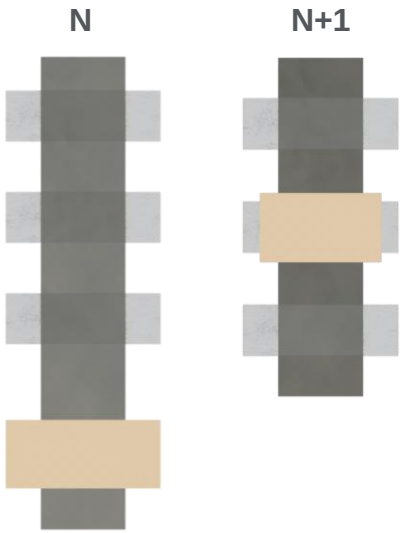
Source: Mark Liu and H.-S. Philip Wong, IEEE Spectrum, March 28, 2024. https://spectrum.ieee.org/trillion-transistor-gpu

Materials Engineering Now Critical to Logic Density Scaling

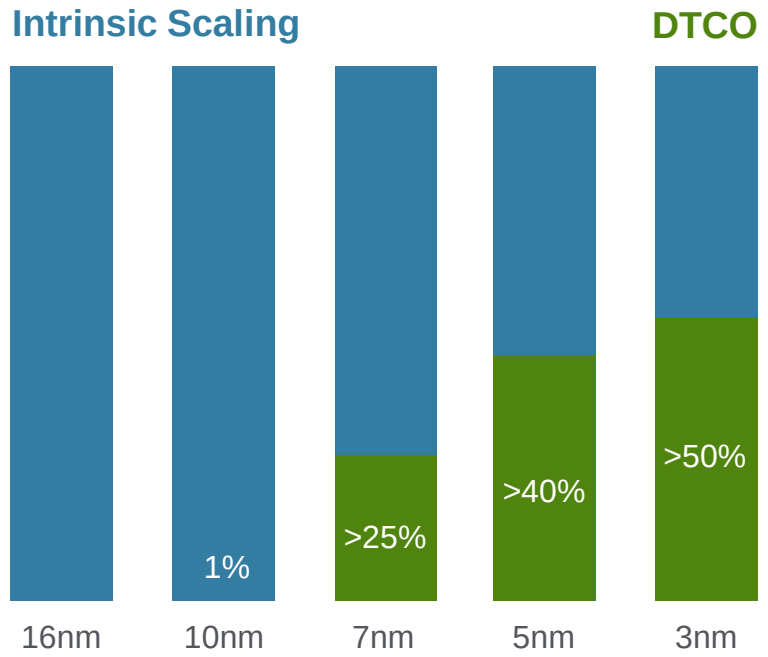
Intrinsic Scaling
= lithography



DTCO = design technology co-optimization with materials engineering

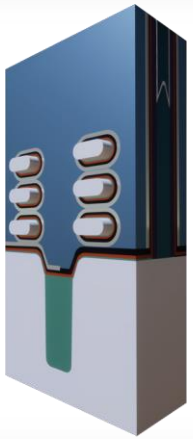


Contribution to Logic Density Scaling



Source: M. Liu/tsmc, ISSCC 2021

New Ways to Increase Logic Density + Improve Power and Performance



GATE-ALL-AROUND

Increases logic density by 10-30% vs FinFET at same lithography; reduces power by up to 30%

~$1B in incremental SAM per 100k WSPM vs FinFET

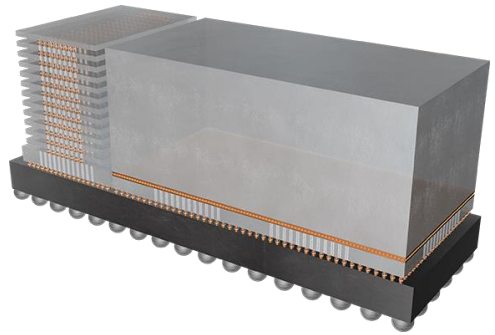
Expect ~50% SAM share

BACKSIDE POWER

Increases logic density by 6-30% at same lithography; reduces power by 3-25%

~$1B in incremental SAM per 100k WSPM vs frontside power

Expect ~50% SAM share



HETEROGENEOUS INTEGRATION

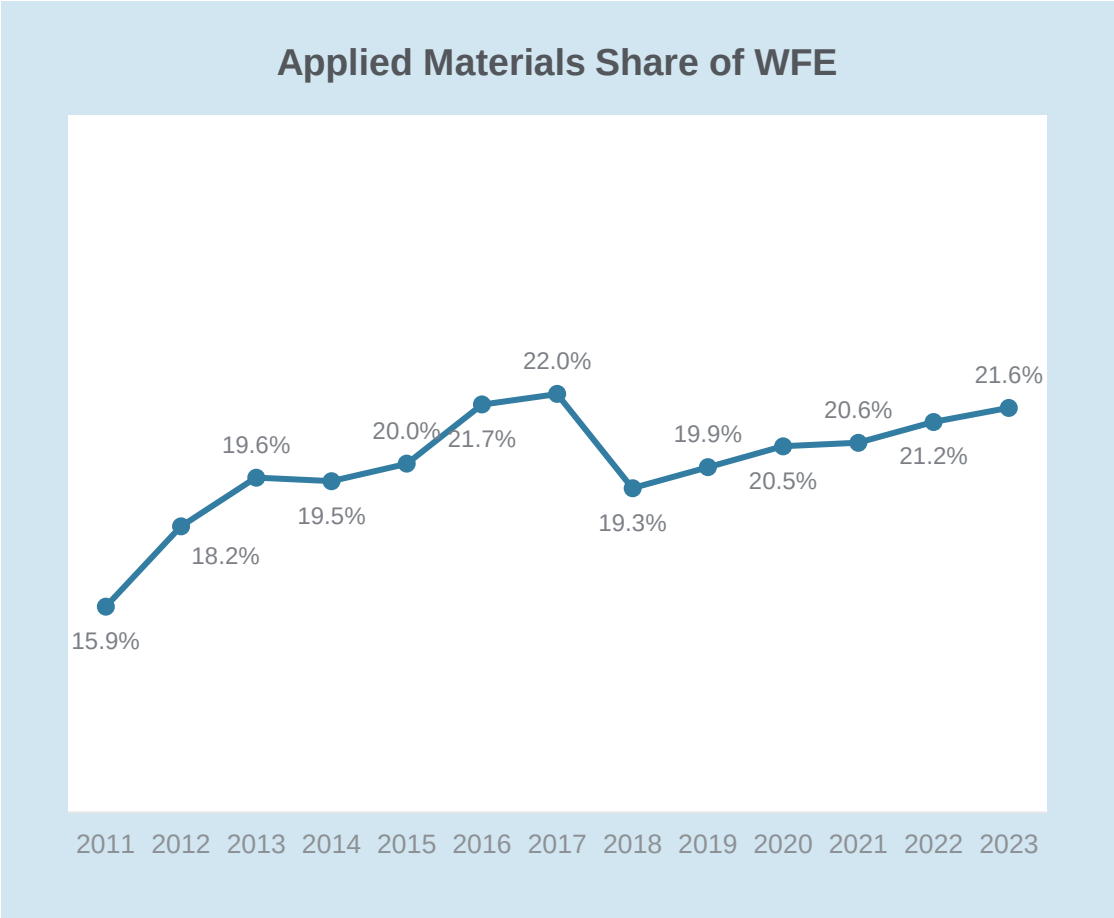
Enables volumetric scaling of logic and memory for “system in package” designs

~$1.1B rev in FY23

Expect ~50% SAM share

Summary

- WFE spending has tracked or exceeded semiconductor growth since 2015
  - » 2023 WFE $95.7B, +1%
  - » Applied outperformed WFE in each of past 5 years
- Materials engineering ~1/2 of WFE market; Applied is #1
- Better AI depends on materials engineering inflections across logic, DRAM and advanced packaging
- Applied expects to outgrow the WFE market through materials engineering leadership
  - » Broadest portfolio of technologies for unit process, co-optimized and integrated solutions



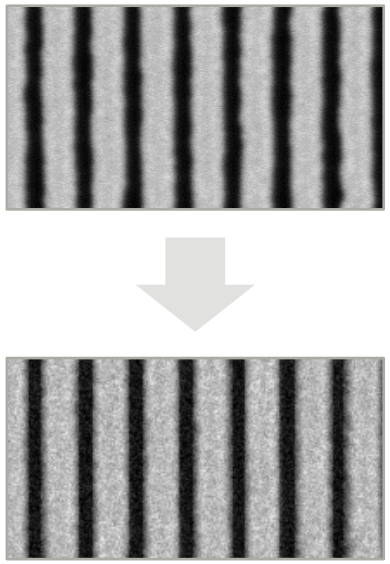
Source: Gartner (2011-19), TechInsights (2020-23), Applied Materials analysis. Baseline year of 2011 is when Applied Materials acquired Varian Semiconductor Equipment Associates, Inc.

Q&A

Additional Material

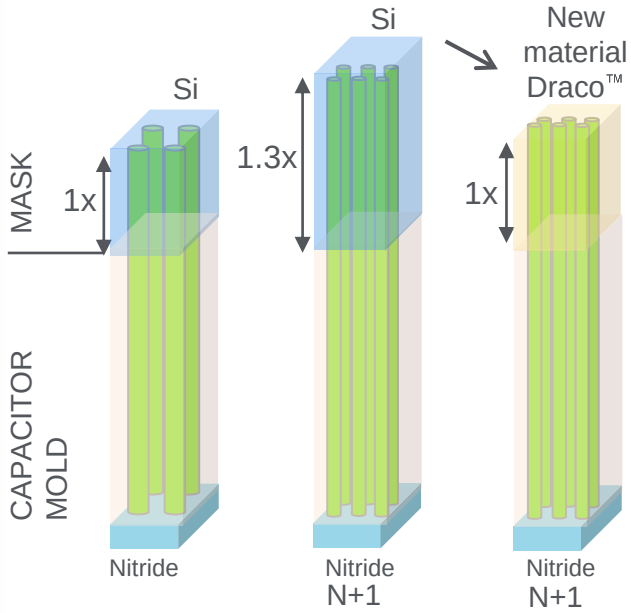
APPLIED MATERIALS®
make possible

Co-optimized Solution Examples



EUV line-space patterning

Pioneer CVD film
+ Sym3 Y Magnum etch
+ PROVision eBeam metrology



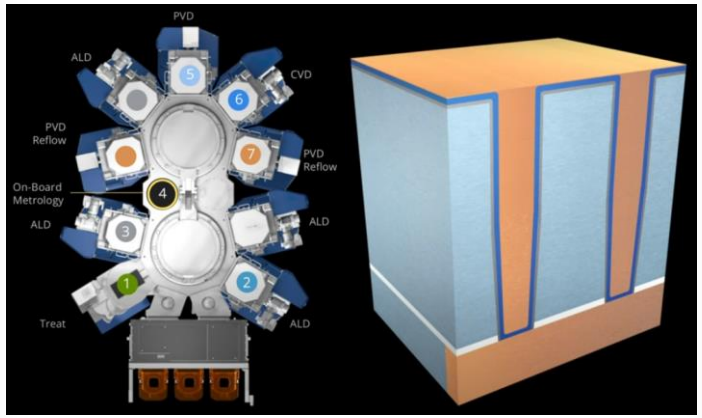
DRAM capacitor patterning

Draco CVD film
+ Sym3 Y etch
+ PROVision eBeam metrology

HBM through-silicon vias

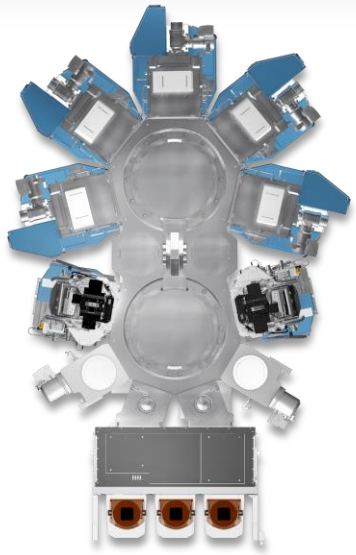
Invia 2 CVD liner
+ Ventura 2 PVD

Integrated Materials Solution Examples



Copper wiring in EUV layers

Barrier-free vias
47% ↓ via resistance

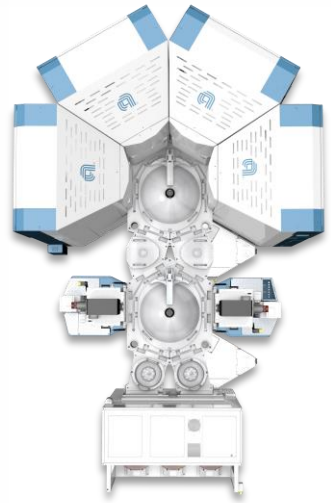


Endura Ioniq™ W

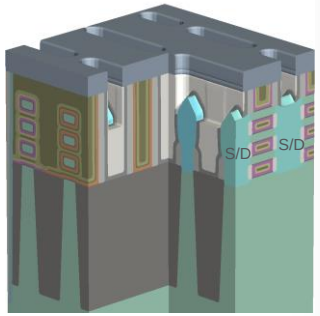
PVD W liner
and CVD W fill

3nm transistor contacts

Pure metal contacts
~40% ↓ contact resistance



Centura Prime Epi



Source-drain epitaxy

GAA selective epitaxy

Silicon gate channel engineering for optimal power and performance

IMS™ Represented ~30% of Semi Systems Revenue in FY23 (vs ~20% in FY19)

Source: Applied Materials analysis

GLOSSARY: Materials Engineering and Other Technologies from Applied

MATERIALS ENGINEERING

Create and Deposit	• **Deposition:** Depositing a thin layer of insulating material (dielectric) or conductive material (metal) onto a substrate. • **Epitaxy (Epi):** Growing a monocrystalline film on a lattice structure and orientation identical to the substrate. • **Chemical Vapor Deposition (CVD):** Depositing a thin film of dielectric material by exposing the substrate to one or more volatile precursors, which react and/or decompose on the substrate's surface. Includes **Atomic Layer Deposition (ALD)** whereby material can be deposited one atomic layer at a time. • **Physical Vapor Deposition (PVD):** Depositing metal by directing ions at a target of pure material to coat a substrate. • **Plating:** Depositing metals contained in a solution onto a charged substrate. • **Selective Deposition:** Occurring only along desired surfaces.
Shape and Remove	• **Etch:** Removing material through a chemical reaction or physical bombardment. The process can be performed using liquid-phase (wet) etchants or under vacuum (dry) typically using a plasma to generate gas-phase reactants. • **Selective Removal:** Removing a target material while leaving other materials in place. • **Pattern Shaping:** Precisely removing dielectric films used in patterning processes to create denser patterns or correct defects. • **Planarization:** Making an uneven wafer surface flat using chemical mechanical planarization (CMP).
Modify	• **Ion Implantation (Implant):** Using intense electrical fields to accelerate ions and penetrate the surface of the wafer, thereby changing the electrical characteristics of the semiconductor material. • **Thermal (Anneals):** Using high temperatures to repair defects in crystal structures or induce phase changes.
Connect	• **Advanced Packaging:** Using front-end wafer fab equipment tools and advanced substrates to connect a variety of chips using increasingly small contacts and wires to increase integration, reduce power and increase performance -- of both chips and systems.

PROCESS CONTROL

Analyze	• **Optical Inspection:** Examining wafers at optical resolution to detect the presence of particles and defects between process steps. • **eBeam Defect Review:** Examining suspected defects at electron beam resolution to see and classify defects and root-cause process issues. • **eBeam Inspection:** Using electron beam technology to detect and identify defects that cannot be detected by optical inspection. • **eBeam Metrology:** Using electron beam technology to measure critical structures including buried structures with nanometer precision. • **CD-SEM:** Calibrating lithography systems by using electron beam technology to measure the critical dimensions of patterns in photoresist.

“Materials Magic” – Fun Facts

Early ICs only used about 8 elements from the periodic table.

Today, more than 25 elements are combined in 100 different ways using Applied Materials’ equipment.

To obtain ultra-high film purity, Applied's Endura deposition system can create a vacuum level of 10^{-11} atmospheres.

That’s about the same vacuum level at 400km above the earth’s surface, or at the orbit of the International Space Station.

To create the transistors on a 300mm wafer, Applied’s etch chambers drill a trillion contact holes, each a thousand times finer than a human hair.

That’s 10 times the number of stars in the Milky Way.

Applied’s CMP systems can smooth the surface of 300mm silicon wafers to a variation of just 5 nanometers.

That’s like a lawn mower that can cut every blade of grass on a soccer field to a height that varies by just the width of a human hair.

To create low resistance contacts, Applied’s laser anneal system heats the surface of a silicon chip to over 1,000°C in less than a millisecond.

That’s approximately the temperature of molten lava.

Applied’s wafer inspection systems can find and identify a defect the size of only a few nanometers on a wafer.

That’s like spotting a single ant on Earth from outer space, and then identifying its species within seconds.

Source: Applied Materials analysis


APPLIED
MATERIALS®
make possible