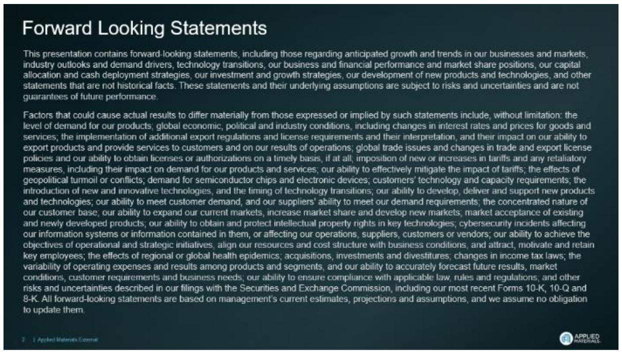
Logic Master Class

PREPARED REMARKS | April 8, 2026

MASTER CLASS April 8, 2026

Leading the Future of Logic with Materials-Enabled Scaling



Forward Looking Statements

This presentation contains forward-looking statements, including those regarding anticipated growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, our business and financial performance and market share positions, our capital allocation and cash deployment strategies, our investment and growth strategies, our development of new products and technologies, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance.

Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: the level of demand for our products; global economic, political and industry conditions, including changes in interest rates and prices for goods and services; the implementation of additional export regulations and license requirements and their interpretation, and their impact on our ability to export products and provide services to customers and on our results of operations; global trade issues and changes in trade and export license policies and our ability to obtain licenses or authorizations on a timely basis, if at all; imposition of new or increases in tariffs and any retaliatory measures, including their impact on demand for our products and services; our ability to effectively mitigate the impact of tariffs; the effects of geopolitical turmoil or conflicts; demand for semiconductor chips and electronic devices; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; our ability to develop, deliver and support new products and technologies; our ability to meet customer demand, and our suppliers' ability to meet our demand requirements; the concentrated nature of our customer base; our ability to expand our current markets, increase market share and develop new markets; market acceptance of existing and newly developed products; our ability to obtain and protect intellectual property rights in key technologies; cybersecurity incidents affecting our information systems or information contained in them, or affecting our operations, suppliers, customers or vendors; our ability to achieve the objectives of operational and strategic initiatives, align our resources and cost structure with business conditions, and attract, motivate and retain key employees; the effects of regional or global health epidemics; acquisitions, investments and divestitures; changes in income tax laws; the variability of operating expenses and results among products and segments, and our ability to accurately forecast future results, market conditions, customer requirements and business needs; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our filings with the Securities and Exchange Commission, including our most recent Forms 10-K, 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

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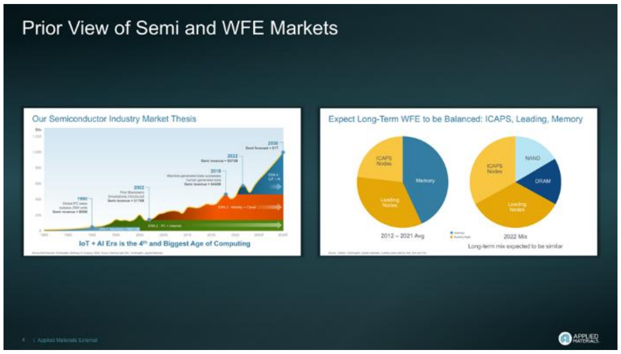
MASTER CLASS April 8, 2026

Welcome

Michael Sullivan
Corporate Vice President
Head of Investor Relations

- Hello and welcome back to the Applied Materials Master Class Series.
- I'm Mike Sullivan, head of investor relations at Applied.
- Before we begin, I'd like to give you an update on our semiconductor and equipment market thesis which sets the stage for the initial topics we've chosen for this year's master class series.



Prior View of Semi and WFE Markets

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- Applied has long expected AI to become the fourth major growth wave for the industry.
- Several years ago, forecasters expected the semiconductor industry to reach $1 trillion dollars by 2030.
- At the time, we expected the WFE market mix to be around 1/3 leading-edge foundry-logic, 1/3 ICAPS—which is non-leading-edge logic and specialty devices—and 1/3 memory, with memory evenly split between DRAM and NAND.

AI Accelerating Semiconductor Demand

NOW:
AI Intelligent Cloud

FUTURE:
AI Intelligence Everywhere!

Semiconductor industry revenues can potentially reach

$1T

this year

- Today, forecasters see the trillion-dollar market arriving as early as this year driven by accelerating demand for data center AI.
- As a result, we believe the WFE industry is diverging.

WFE Market Outlook

FASTEST GROWING AREAS OF THE MARKET

	INFLECTIONS
Leading-Edge Foundry/Logic	Gate-all-around transistors Backside power delivery
DRAM	$4F^2$ 3D DRAM
Advanced Packaging	High-bandwidth memory (HBM) Hybrid bonding Panel substrates

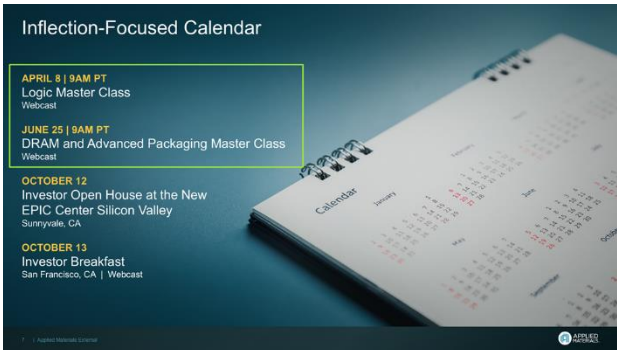
APPLIED MATERIALS

#1 Process Equipment Company in All Three Markets

SLOWER GROWING AREAS

NAND	Increased layers Technology transitions
ICAPS	Compound semi (SiC, GaN) Photonics

- The markets that enable data center AI are growing much faster than the market average, and the rest are growing slower.
- The faster-growing markets are leading-edge foundry-logic—which consists of transistors and on-chip wiring—along with DRAM and advanced packaging.
- The slower growing markets are NAND memory and ICAPS.
- And that brings us to the first two events in this year's Master Class series, which are designed to explain the technology inflections in the fastest growing areas of the market.



Inflection-Focused Calendar

APRIL 8 | 9AM PT
Logic Master Class
Webcast

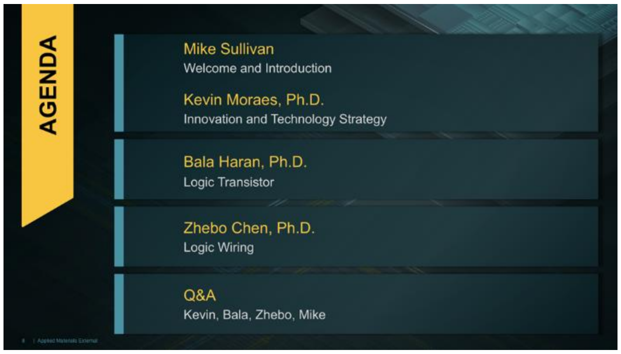
JUNE 25 | 9AM PT
DRAM and Advanced Packaging Master Class
Webcast

OCTOBER 12
Investor Open House at the New EPIC Center Silicon Valley
Sunnyvale, CA

OCTOBER 13
Investor Breakfast
San Francisco, CA | Webcast

- Today's event is focused on transistors and on-chip wiring.
- And in June, we'll share the DRAM and advanced packaging roadmap.

- Later this year, during SEMICON West week, we hope you'll join us for an open house event at the new EPIC Center in Silicon Valley, California.
- We also hope to see you at our SEMICON West investor breakfast in San Francisco.



AGENDA

Mike Sullivan
Welcome and Introduction

Kevin Moraes, Ph.D.
Innovation and Technology Strategy

Bala Haran, Ph.D.
Logic Transistor

Zhebo Chen, Ph.D.
Logic Wiring

Q&A
Kevin, Bala, Zhebo, Mike

- In today's meeting, we're going to cover 5 topics.
- First, Dr. Kevin Moraes will help you understand our inflection-focused innovation strategy. He'll do this by summarizing our technology portfolio and how we connect these technologies to create co-optimized and integrated solutions that help accelerate the roadmaps for our customers.
- Next, Dr. Bala Haran will summarize the industry's transistor roadmap, the key materials engineering challenges in gate-all-around transistors, and the solutions we're using to address them.
- Then, Dr. Zhebo Chen will discuss the on-chip wiring roadmap for advanced foundry-logic and the materials engineering solutions the industry increasingly needs.
- And finally, all of us will address your questions.
- And with that introduction, I'd like to hand the meeting over to Kevin.

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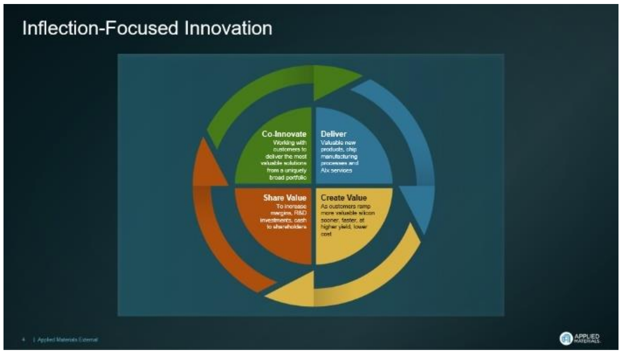
Innovation and Technology Strategy

Kevin Moraes, Ph.D.
Corporate Vice President
Strategy and Marketing
Semiconductor Products Group

APPLIED MATERIALS

- Thanks Mike.
- I'm Kevin Moraes, head of marketing and strategy for Applied's Semiconductor Products Group.
- Mike just outlined how AI is reshaping the industry and where the fastest growth is occurring.
- I'll start by explaining how our strategy and technology portfolio are designed to address those inflections.



Inflection-Focused Innovation

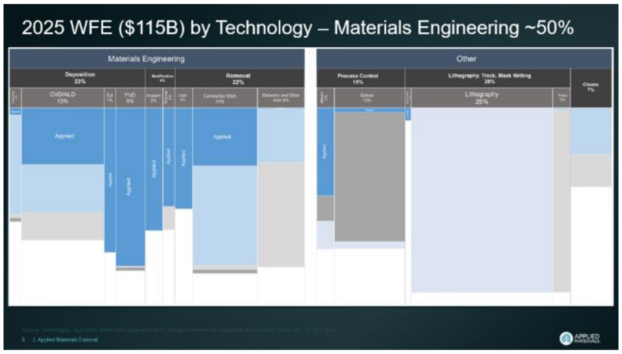
Co-Innovate Working with customers to deliver the most valuable solutions from a uniquely broad portfolio

Deliver Valuable new products, chip manufacturing processes and AIx services

Share Value To increase margins, R&D investments, cash to shareholders

Create Value As customers ramp more valuable silicon sooner, faster, at higher yield, lower cost

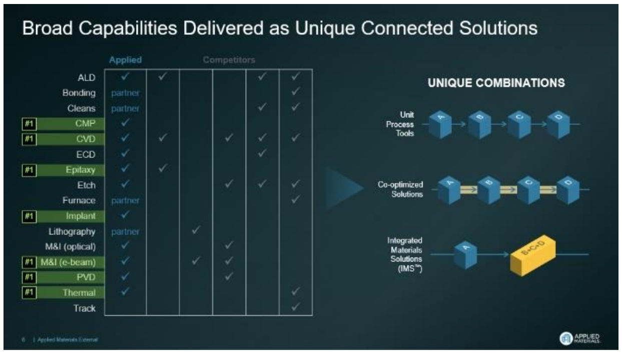
- At Applied, our strategy is called inflection-focused innovation.
- We work side-by-side with the world's leading semiconductor manufacturers, targeting the next three-plus nodes of future semiconductor technology—often a decade ahead of production.
- We aim to identify and solve the hardest materials engineering challenges early.
- We do this by combining our broad portfolio of unit process systems, co-optimized solutions and integrated solutions to help create the semiconductors and systems of the future.
- These solutions deliver value to our customers in the form of faster and more energy-efficient chips which is what the AI ecosystem needs most.
- We also deliver advanced services that help our customers ramp these new technologies faster and at higher levels of performance, reliability and yield.
- Together, our products and services create value for our customers.
- And we share in the value we create to increase profitability so that we can invest even more in co-innovating with our customers as well as reward our shareholders.



2025 WFE ($115B) by Technology – Materials Engineering ~50%

- This chart is a summary of the Wafer Fab Equipment (WFE) industry, with materials engineering on the left, and other technologies on the right.
- Applied is the leader in the three key categories of materials engineering: materials deposition, materials modification, and materials removal.
- Applied is #1 in deposition overall, and #1 in CVD, PVD, and epitaxy.
- Applied is also #1 in materials modification, both overall and in all three categories of ion implantation, thermal processes and treatments.

- In materials removal, Applied is #1 in CMP.
- And within the broader etch segment, Applied leads in conductor etch in the fast-growing DRAM and leading-edge foundry-logic markets.
- In process control, Applied is #1 in eBeam metrology, which is becoming increasingly important as the industry moves to 3D architectures.
- This is a technology we use to make massive measurements—across the wafer and within the wafer—to optimize and accelerate our materials engineering solutions.



Broad Capabilities Delivered as Unique Connected Solutions

	Applied	Competitors				
ALD	✓	✓			✓	✓
Bonding	partner					✓
Cleans	partner				✓	✓
#1 CMP	✓					
#1 CVD	✓	✓		✓	✓	✓
ECD	✓				✓	
#1 Epitaxy	✓	✓				
Etch	✓			✓	✓	✓
Furnace	partner					✓
#1 Implant	✓					
Lithography	partner		✓			
M&I (optical)	✓			✓		
#1 M&I (e-beam)	✓		✓	✓		
#1 PVD	✓			✓		
#1 Thermal	✓					✓
Track						✓

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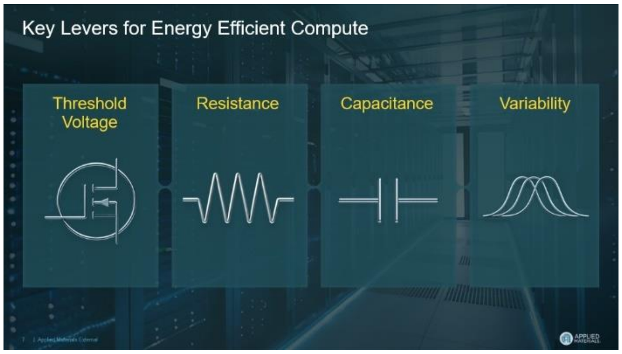
- What all of this means is Applied has the industry's broadest portfolio of technologies needed to build transistors, on-chip wiring and advanced packaging.
- And we deliver our materials engineering capabilities in three complementary ways.
- First, our unit process systems perform individual steps on the wafer.
- Our customers lead the integration of these steps into the overall semiconductor manufacturing sequence.
- Our co-optimized solutions perform multiple adjacent or non-adjacent steps on the wafer in different systems, and Applied ensures that the steps we've co-optimized are proven to meet the customer's integration requirements.
- Finally, our integrated systems perform multiple consecutive steps in a single high-vacuum platform.
- This integration also protects delicate semiconductor materials and structures from cleanroom contamination.
- Applied ensures that all of these consecutive steps meet the customer's integration requirements.
- Around 30% of Applied's systems revenue comes from integrated systems.
- In the AI data center, system performance-per-watt has become the defining metric.
- At the chip level, there are four key levers we can drive to improve performance-per-watt.



Key Levers for Energy Efficient Compute

Threshold Voltage

Resistance

Capacitance

Variability

- First, we can reduce the transistor threshold voltage.
- Threshold voltage is the minimum voltage needed to turn a transistor from the off state to the on state.
- Reducing transistor threshold voltage means the transistor turns on more easily and switches more quickly—resulting in higher performance.
- Second, we can reduce resistance, in both transistors and wiring.
- Resistance restricts the flow of electricity which limits performance and creates heat that needs to be dissipated from the chip and system.
- In fact, one of the biggest costs in running a data center is cooling.
- Third, we can reduce capacitance.
- Capacitance is the amount of electric charge that must be moved when signals switch directions—whether in transistors or in the wiring that connects them.
- Think of it like a bucket that must be filled and emptied every time a signal changes.
- A smaller bucket takes less charge—and less time—to fill and empty.
- Lower capacitance means less energy is needed for signals to switch, enabling faster, more energy-efficient operation across the chip.
- Fourth, we can reduce variability.
- Variability refers to small differences in behavior caused by differences in materials composition or geometry.
- For example, variability can cause some components in a circuit to operate more slowly than others, forcing the entire system to run slower and consume more energy per operation.
- Now I'd like to invite Dr. Bala Haran to discuss how we put all of our technology to work in helping our customers drive the transistor roadmap. Bala?

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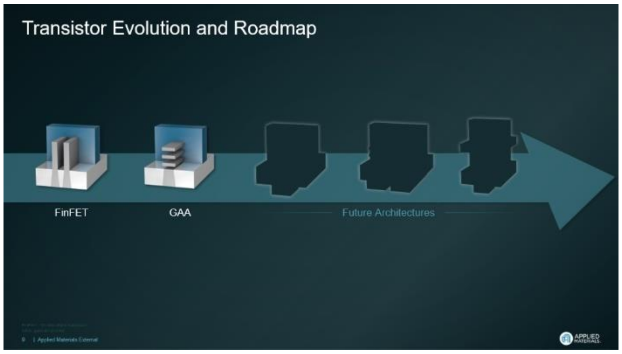
Logic Transistor

Bala Haran, Ph.D.
Corporate Vice President
Integrated Materials Solutions
Semiconductor Products Group

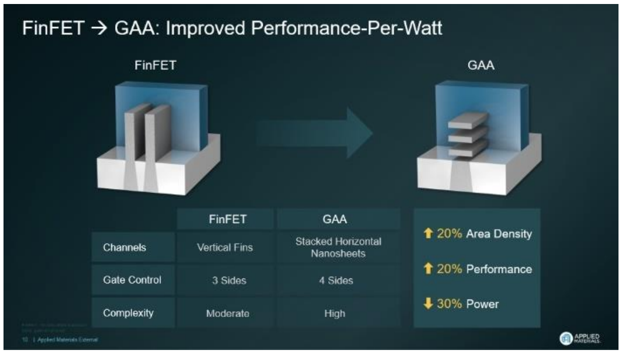
- Thanks, Kevin. I’m Bala Haran, Vice President of Integrated Materials Solutions™.
- I’ve spent much of my career integrating semiconductor process technologies at IBM.
- At Applied, I’ve had the honor of working closely with all of the leading chipmaking and semiconductor companies to help drive the industry’s roadmap.
- Let me zoom out to the big picture of what’s changing across the industry.
- With the AI boom, we see more hyperscalers and startups designing AI models and AI accelerators to gain differentiation.
- But here’s a key point: Despite rapid change in models and accelerators, the foundation is still transistors and wiring.
- By improving the transistors and wiring, we can make all of these chips and models work even better.
- Now let’s focus on the transistor.
- A leading-edge GPU for AI applications can use over 200 billion transistors.
- These transistors can consume between one-half to two-thirds of chip power, with the balance consumed by wiring.



Transistor Evolution and Roadmap

- The industry has invented a number of different transistor architectures, each designed to allow more transistors to fit in a smaller space while switching faster and consuming less power.
- Today, the FinFET transistor is still the workhorse of most AI GPUs.
- But the need for higher transistor counts, higher performance and lower power is driving the transition from FinFET to gate-all-around.

- I'll take a moment to talk about how FinFET and gate-all-around (GAA) transistor architectures affect area, performance and power scaling.

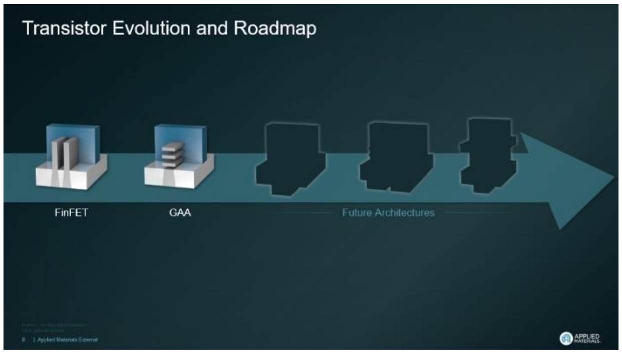


FinFET → GAA: Improved Performance-Per-Watt

	FinFET	GAA
Channels	Vertical Fins	Stacked Horizontal Nanosheets
Gate Control	3 Sides	4 Sides
Complexity	Moderate	High

↑ 20% Area Density
↑ 20% Performance
↓ 30% Power

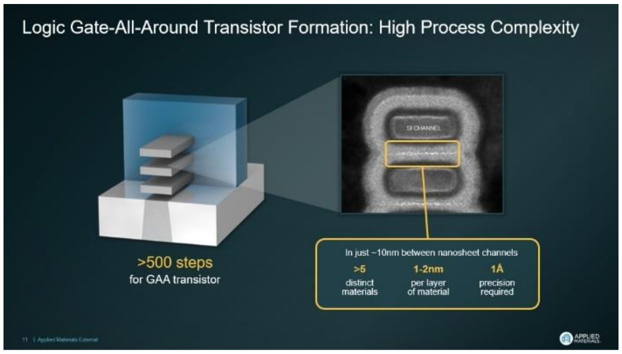
- In the FinFET architecture, logic density is a function of how closely we can pack the vertical fins in a lateral space.
- The GAA transistor takes logic density scaling to a new level by changing the layout of the silicon channels.
- Instead of the fins in FinFET transistors, GAA transistors have silicon nanosheets that are stacked vertically, which allows more of them to be packed into a given area.
- Density versus FinFET can be increased by as much as 20% at the same lithography.
- The GAA transistor architecture also offers another key benefit versus FinFET.
- In FinFET transistors, the fins are surrounded on three sides by the gate, which controls threshold voltage and leakage.
- In GAA transistors, the gate now surrounds the silicon channels on all sides.
- This further improves threshold voltage control and leakage current.
- Moreover, the channel width can be smoothly adjusted—giving chip designers an extra "tuning knob" to balance performance and power.
- As a result, performance can improve by up to 20% at the same power—or we can achieve the same performance while using 30% less power.



Transistor Evolution and Roadmap

- While the first chips using GAA transistors are just arriving in the industry, we are already working on future extensions of the technology that will bring more performance gains.

- I’ll touch more on these later.
- So the benefits of GAA transistors are compelling.
- But the complexity is also extreme and mostly solved by breakthroughs in materials engineering and eBeam process control.


Logic Gate-All-Around Transistor Formation: High Process Complexity

>500 steps
for GAA transistor

In just ~10nm between nanosheet channels

>5	1-2nm	1Å
distinct materials	per layer of material	precision required

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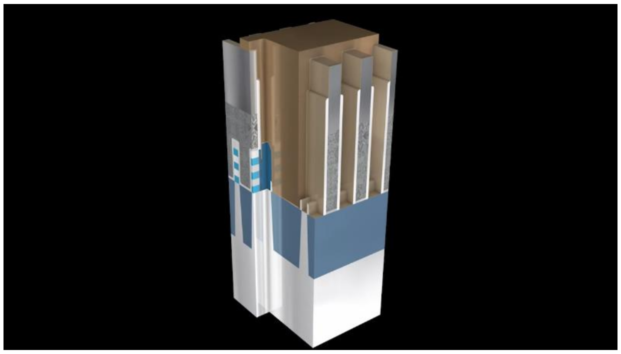
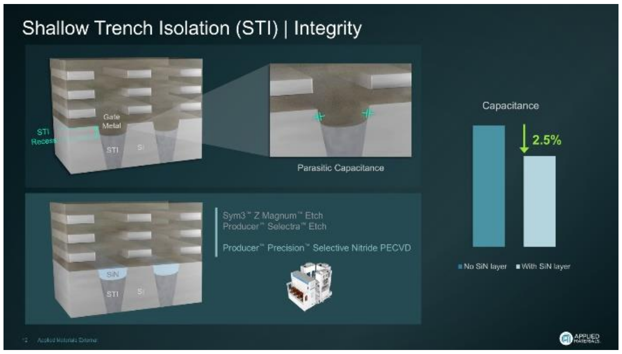
- Building GAA transistors requires hundreds of process steps.
- And the dimensions are like nothing the industry has seen before.
- For example, the space between the silicon nanosheet channels—which is determined by deposition and not lithography—is as small as 10 nanometers.
- Imagine the width of a single human hair divided into 10,000 evenly spaced slices.
- That gives you a feel for how small the space between the gate-all-around nanosheets is.
- Now imagine that between these slices, you need to deposit five different materials—with atomic layer control—with perfect uniformity across the length of a 300-millimeter wafer.
- This is just one example of why GAA materials engineering is so challenging.


(Animation)

- Next, let’s view an animation that highlights a number of the key steps used to build the gate-all-around transistors.
- We start with a blank wafer.
- Then, we use epitaxy to deposit extremely thin, alternating layers of silicon and silicon germanium.
- The silicon will become the transistor channels, and the silicon germanium is sacrificial—there temporarily to support the transistor channels we are building.

- Next, we perform shallow trench isolation.
- We etch through the silicon and silicon germanium layers into the wafer, defining the width of each transistor and creating a shallow trench within the wafer.
- Then we use deposition to fill the trench with an insulating material called silicon oxide.
- Next, we again etch through the silicon and silicon germanium layers, setting the length of each transistor.
- Next, we etch spaces at the ends of the silicon channels which define the source/drain regions where current enters and exits the channels when the transistor is in the on state.
- Next, we use epitaxial deposition to selectively fill the source/drain regions with special material that creates optimal electron and hole mobility which is critical to performance.
- Next the sacrificial silicon germanium is selectively etched away, leaving only the silicon channels.
- Next, we apply a special treatment to the silicon channels to make sure they are perfectly smooth.
- At this point, the transistor can carry current—but it still can't be controlled.
- We next deposit several layers of material around the silicon channels to create the gate stack which acts like a switch that turns the transistor on and off.
- The gate stack is made up of multiple atomic-scale layers, engineered to work together as a system to precisely control the transistor.
- Surrounding the silicon channels are dielectric layers that provide strong electrostatic control of the channel.
- And we treat the dielectric layers to improve the stability of the gate stack.
- Then atomic layer deposition is used to surround the dielectric layers with a metal gate that controls whether the transistor is on, allowing current to flow through the nanosheets.
- Now you know how GAA transistors are built.
- We'll next revisit some of the key steps and explain the products Applied Materials has developed to help our customers build the best transistors for energy-efficient AI computing.
- These products are among many that have earned Applied Materials the #1 position in GAA transistor materials engineering, with around 50% share of the industry's investments.

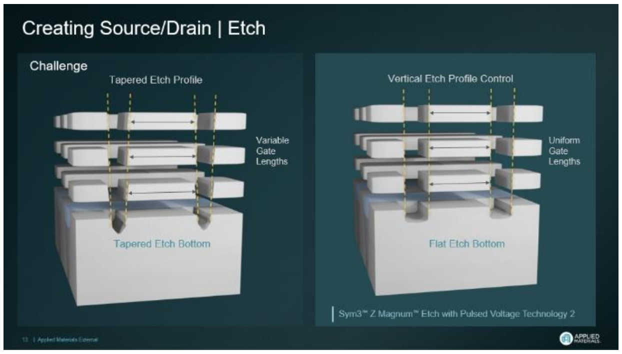


Shallow Trench Isolation (STI) | Integrity

Sym3™ Z Magnum™ Etch
Producer™ Selectra™ Etch

Producer™ Precision™ Selective Nitride PECVD

- Let’s return to shallow trench isolation—also called STI.
- To pack hundreds of billions of transistors on a chip, we need to shrink the distance between transistors to the smallest number of nanometers possible.
- Without isolation, electric charge can leak between the transistors, increasing capacitance—and degrading transistor speed and wasting power.
- We use Sym3™ Z Magnum™ to etch an isolation trench, then fill it with insulating silicon oxide.
- However, some downstream processes are oxide-selective.
- This means they preferentially etch silicon oxide, which can unintentionally recess the isolation.
- That’s why we’ve launched an innovative solution called Producer™ Precision™ Selective Nitride to build robust protection for the silicon oxide STI.
- We start by precisely etching the silicon oxide to the desired height.
- We then fill the cavities with silicon nitride using our Producer™ Precision™ platform.
- This silicon nitride can withstand the oxide-selective downstream processing without recessing.
- A special materials engineering challenge is that the silicon nitride needs to be selectively deposited only on the recessed silicon oxide in the isolation trench.
- Producer™ Precision™ is the industry’s first selective bottom-up silicon nitride solution—ensuring high-quality silicon nitride is deposited only where it’s useful and nowhere else.
- The end result is high-quality GAA shallow trench isolation that preserves its isolation integrity and reduces capacitance to increase transistor speed and power efficiency.



Creating Source/Drain | Etch

Sym3™ Z Magnum™ Etch with Pulsed Voltage Technology 2

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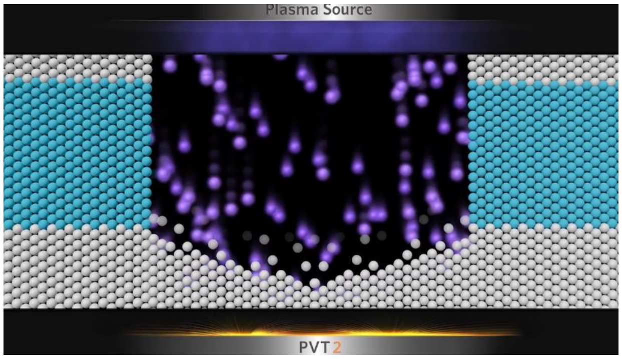
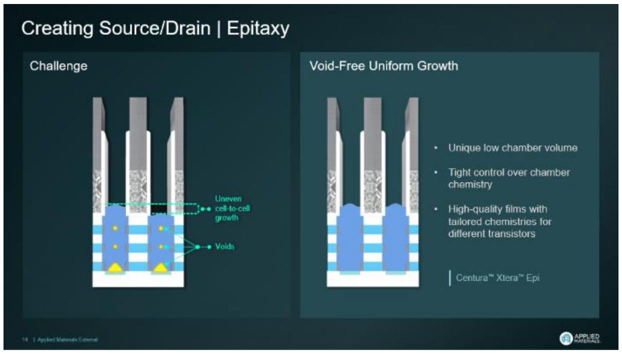
- Next, let’s take a closer look at the source/drain engineering, beginning with the etch step used to form the source/drain cavities.
- These cavities must be extremely narrow but also deep enough to surround all three of the silicon nanosheets.
- Traditional etchers create V-shaped cavities that are wide at the top and narrow at the bottom.
- However, creating the best GAA transistors demands etching perfectly rectangular cavities with perfectly flat bottoms.
- The first benefit of these shapes is that each silicon channel is made to the same length, which reduces variability in performance.
- The second benefit is that the flat bottoms are ideal for the subsequent, selective epitaxy steps.
- Applied developed the Sym3™ Z Magnum™ etch system to enable these shapes using a breakthrough called Pulsed Voltage Technology—or PVT.
- PVT has helped Applied Materials to become the #1 provider of conductor etch systems in both leading-edge foundry-logic and DRAM.
- The first PVT is excellent for 2nm and above gate-all-around transistors and also DRAM conductor etch applications.



(Animation)

- Our newest PVT2 technology enables high-quality GAA transistors beginning at sub-2nm nodes.
- PVT2 tunes etch ion energies and angles to form ideal vertical sidewalls, shape bottom corners, and create uniformly deep and flat bottoms.

- It also delivers near-wafer plasma control, so etching produces predictable results even at great depths.
- Next, let’s discuss how we create highly conductive films to transport charges from the silicon channels.



Creating Source/Drain | Epitaxy

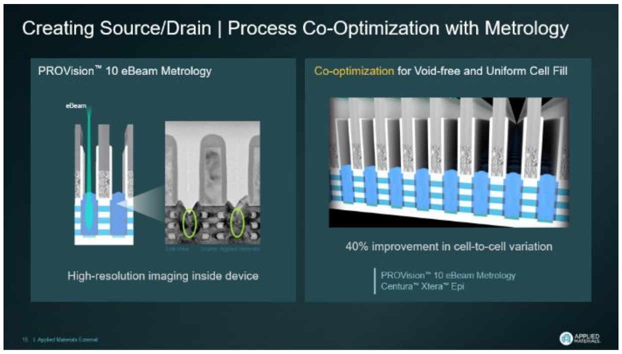
Challenge

Void-Free Uniform Growth

- Unique low chamber volume
- Tight control over chamber chemistry
- High-quality films with tailored chemistries for different transistors

Centura™ Xtera™ Epi

- Within the narrow cavities created by Sym3™ Z Magnum™, we need to grow special films designed to increase electron and hole mobility for optimum transistor performance.
- These films need to be perfectly grown to prevent any voids or defects that can hinder current flow and slow the transistors.
- We developed the Centura™ Xtera™ epitaxy system to grow high-quality films with tailored chemistries for different types of transistors—such as Boron-doped Silicon Germanium in PMOS transistors and Phosphorus-doped Silicon films in NMOS transistors.
- The Xtera™’s uniquely small-volume chamber allows extremely fast chemistry switching, delivering precise control of epitaxial growth.
- The material is selectively grown from the bottom to the top of the trench and prevents growth in unwanted areas—creating the ideal source/drain film needed to carry current.
- By now, you can appreciate how much harder it is to engineer 3D GAA transistors which are full of high-aspect ratio and buried structures.
- That’s why as Kevin mentioned earlier—we co-optimize our processes with leading-edge metrology systems that can “see” deep into these complex 3D structures.



Creating Source/Drain | Process Co-Optimization with Metrology

PROVision™ 10 eBeam Metrology

High-resolution imaging inside device

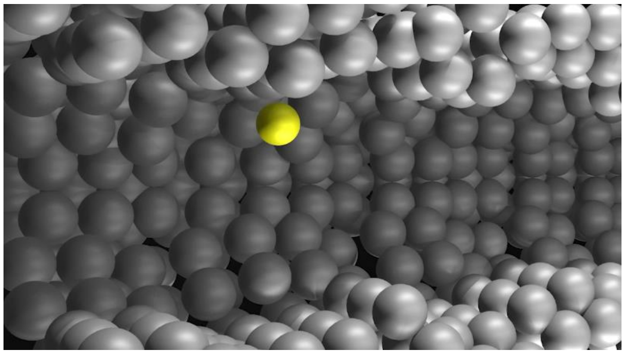
Co-optimization for Void-free and Uniform Cell Fill

40% improvement in cell-to-cell variation

PROVision™ 10 eBeam Metrology
Centura™ Xtera™ Epi

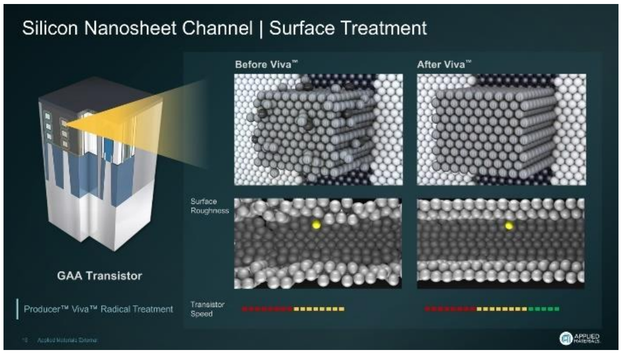
- For example, we co-optimize the Xtera™ epitaxy process with our PROVision™ 10 eBeam metrology system to deliver void-free, high-quality epitaxy for GAA transistor.

- This process-metrology co-optimization increases transistor-to-transistor film uniformity by more than 40%.
- PROVision™ replaces traditional Transmission Electron Microscopy (TEM), which is slow and provides limited data—with fast, high-volume, wafer-level insight.
- It directly scans high-resolution electron beams into complex structures at a variety of energies and depths.
- By collecting back-scattered electrons from deep within the structures, it generates detailed images and precise measurements using advanced algorithms.
- It can take as many as 10,000 measurements across the wafer in an hour, ensuring atomic-scale features are uniform across the entire wafer.
- Having PROVision™ in our portfolio accelerates learning for Applied and our customers—and increases the adoption of Applied's entire process equipment portfolio.
- Now that the source/drain trenches have been formed, let's turn to the gate stack, which is made up of silicon transistor channels, the dielectric layers, and the metal layers.
- The silicon channels are revealed after selective etch has been used to remove the sacrificial silicon germanium.



(Animation)

- Inevitably, etching can leave behind surface roughness and trace germanium on the silicon channels.
- At the atomic scale, even the smallest defects increase resistance and degrade electron mobility.
- It's like being in a supercar driving on a road pitted with potholes—you are forced to slow down.
- To overcome this, we developed the Producer™ Viva™ treatment system.
- Viva™ delivers precisely-controlled energy to the silicon channels.
- It uses a patented architecture to filter out harsh ions from the energy stream.
- What's left are the concentrated neutral radical species of highly reactive atoms that can clean and smooth the surface without damaging it.



Silicon Nanosheet Channel | Surface Treatment

Producer™ Viva™ Radical Treatment

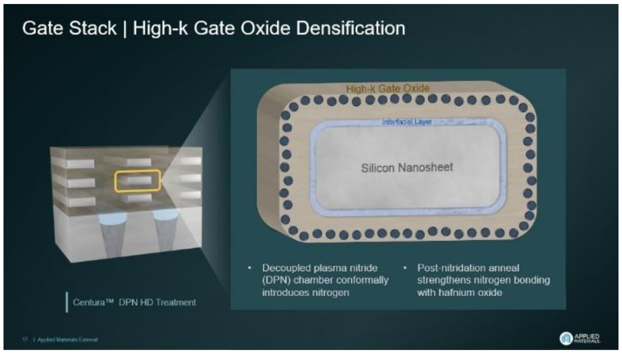
- The result is pristine nanosheet channels and faster, more energy-efficient transistors.

- Treatments like Viva™ are a great example of the materials modification category of wafer fab equipment that Kevin mentioned earlier.

- Materials modification is a category beyond deposition and etch.

- It’s a multibillion-dollar market that is critical to transistor performance and speed—and where Applied has a very strong #1 position.

- Next let’s talk about how we surround the silicon channels with the gate dielectric.



Gate Stack | High-k Gate Oxide Densification

- Decoupled plasma nitride (DPN) chamber conformally introduces nitrogen
- Post-nitridation anneal strengthens nitrogen bonding with hafnium oxide

Centura™ DPN HD Treatment

- It’s important to make pure films with uniform properties since defects, trapped charges and weak chemical bonds can degrade transistor performance.

- To engineer the gate oxide dielectric layer, we developed the Centura™ DPN HD system.

- Centura™ DPN HD integrates two kinds of chambers on the same system.

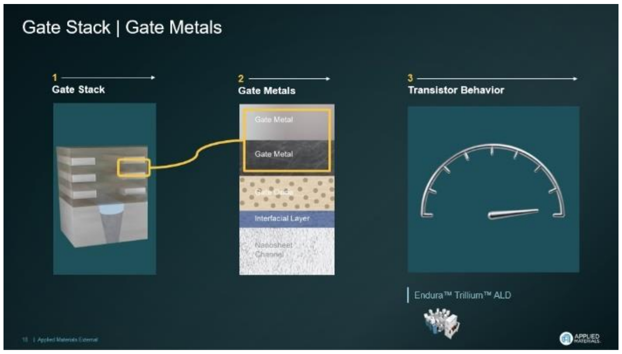
- The high-dose decoupled plasma nitridation chamber injects nitrogen into the dielectric to improve electrostatic control.

- The nitrogen dose is very precisely controlled since having too many nitrogen atoms can cause electrons to scatter.

- The post-nitridation anneal chamber uses carefully controlled heat to help the nitrogen atoms bond with hafnium oxide atoms in the gate oxide.

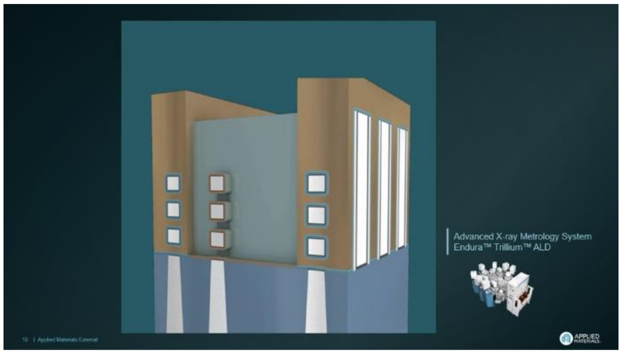
- The stronger bonding network makes the dielectric layer denser and more reliable.

- The result is maximum electrostatic efficiency for faster transistor switching at lower power.



Gate Stack | Gate Metals

- Finally, let's discuss how we deposit the metal gate stack, which is a series of thin, highly engineered layers that work as a system to control the transistor's on and off states.
- We first deposit work-function metals whose electrical properties control the threshold voltage.
- Then, we deposit a fill layer, which uses a low-resistance metal to support faster switching and strong signal integrity.
- A key point is that we can tune the metal gate stack for specific threshold voltages needed in different kinds of systems.
- We have deep expertise in a wide spectrum of metals that have different electrical properties, and this enables us to work with customers to tune process recipes for a wide range of computing products.
- For instance, in AI accelerators, we use lower threshold voltages that put the transistor in the on state more quickly but use more power.
- In smartphones, we use higher threshold voltages that require more time for the transistor to be switched on but reduce leakage power.
- To enable that flexibility, we integrate multiple metal deposition steps in a single innovative solution called the Endura™ Trillium™ ALD system.



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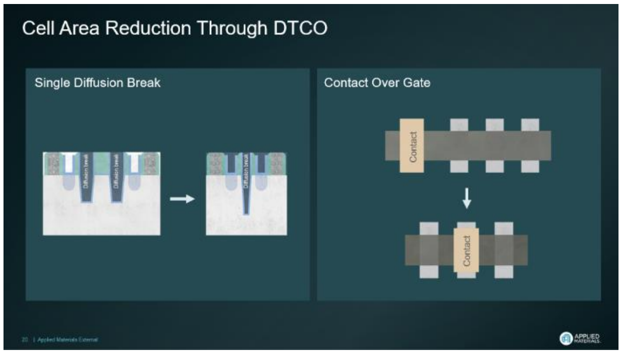
- By integrating multiple metal deposition steps in a single platform, Trillium™ gives designers the flexibility to tune electrical properties—and threshold voltage—across different transistors.
- And it harnesses our leadership in metal ALD technology, delivering angstrom-level thickness control across metal gate stack layers for advanced devices.

- Trillium™ also leverages our proven Endura™ platform, which is the most successful metallization system in the history of the semiconductor industry.
- A key attribute of the Endura™ system is that it creates and maintains an extraordinarily high vacuum, which protects wafers from the impurities in the cleanroom atmosphere.
- This is critical because at gate-all-around nodes, even the slightest contamination can impact transistor performance, power and reliability.
- And remember: in advanced 3D devices like GAA transistors, even small variations can affect threshold voltage, increase leakage power, and increase reliability risk.
- We need precision all the way down to the sub-angstrom level.
- That’s why Trillium™ is co-optimized with an advanced materials metrology system.
- The metrology system uses non-destructive X-ray analysis to rapidly verify gate-metal composition and uniformity without causing any damage to the fragile GAA nanosheets.
- This creates tight, real-time feedback between gate-metal deposition and critical gate-stack measurements.
- The last topic I’ll cover is something we call Design Technology Co-optimization—or DTCO.
- I talked about how as lithographic scaling has slowed, the industry has turned to 3D device designs—like gate-all-around—that stack silicon channels vertically to increase logic density at the same lithography.
- DTCO includes additional ideas for packing more logic into the same area at the same lithography, bringing transistors closer together without sacrificing performance or functionality.

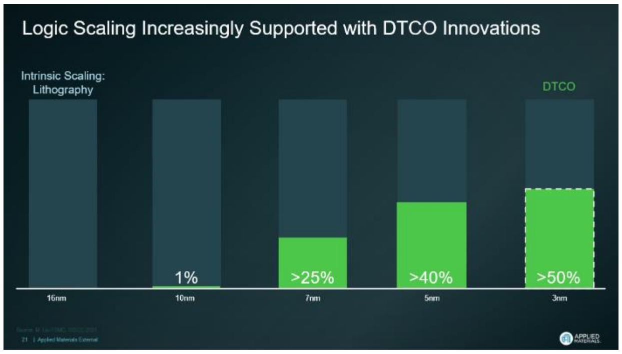


Cell Area Reduction Through DTCO

Single Diffusion Break

Contact Over Gate

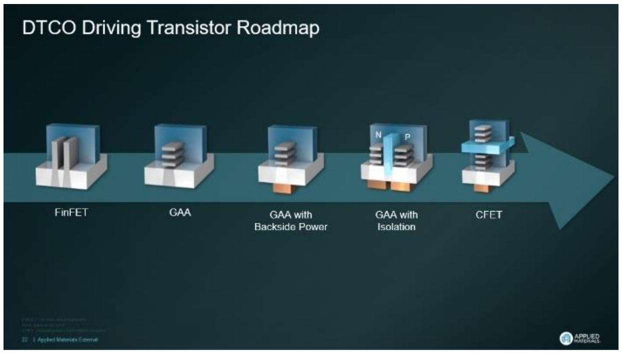
- On the left, we show how designers moved from using a double diffusion break to electrically isolate neighboring transistors to a single diffusion break.
- This saves space and enables more transistors to fit on the same chip.
- On the right, we show another space-saving tactic, whereby designers moved the electrical contact from the side of the transistor to the top, which is called contact over gate.



Logic Scaling Increasingly Supported with DTCO Innovations

- One of our largest customers has said that DTCO techniques drove 25% of scaling at the 7nm node, and 50% of scaling at the 3nm node—at which point DTCO became as important as lithography in increasing logic density.

- In gate-all-around and future generations of transistors and wiring, DTCO continues to play a critical role in logic density scaling.

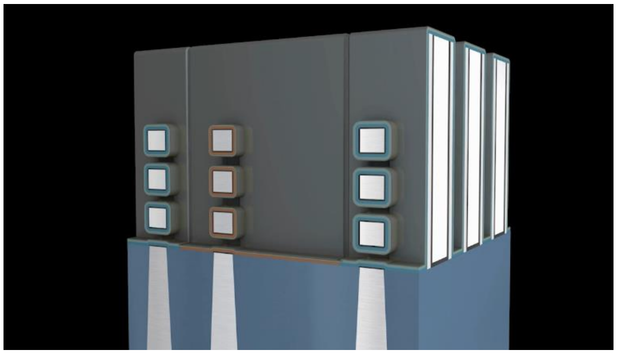


DTCO Driving Transistor Roadmap

- For example, by adding a dielectric isolation wall between pairs of positive, PMOS transistors and negative, NMOS transistors, we can pack more into a smaller space.

- CFET transistors take this further by vertically stacking PMOS and NMOS pairs to increase density even more.

- And as Zhebo will describe, DTCO also extends to wiring innovations like backside power delivery.



(Animation)

- I hope you enjoyed learning about the materials engineering needed to make gate-all-around transistors which are the foundation of all the exciting AI systems that will soon be introduced in the industry.

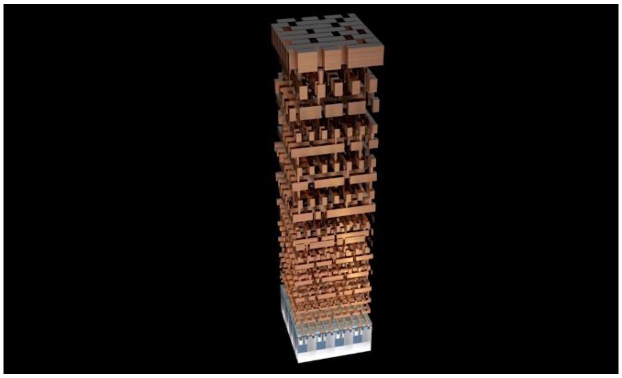
- A final insight I'd like to share with you is that the logic transistor roadmap inflections I described are becoming increasingly important in DRAM as memory architectures grow more logic-like.
- But that's the subject of our next Master Class.
- Now, I'll hand the meeting over to Dr. Zhebo Chen who will take us through wiring—the other major driver alongside transistors for improving chip performance-per-watt. Zhebo?

MASTER CLASS April 8, 2026

Logic Wiring

Zhebo Chen, Ph.D.
Senior Director
Metal Deposition Products
Semiconductor Products Group

- Thanks, Bala.
- I'm Zhebo Chen, Applied's Senior Director for metal deposition products.
- As Bala said, AI chip designers are moving to new 3D transistor architectures, in large part from the desire to pack more transistors onto every chip.
- What you may not know is that wiring increases right along with transistor scaling and density.
- There are two ways to increase wiring to connect more transistors.
- First, we can pack more wires in a given space by making them thinner.
- Second, we can add more wiring layers.



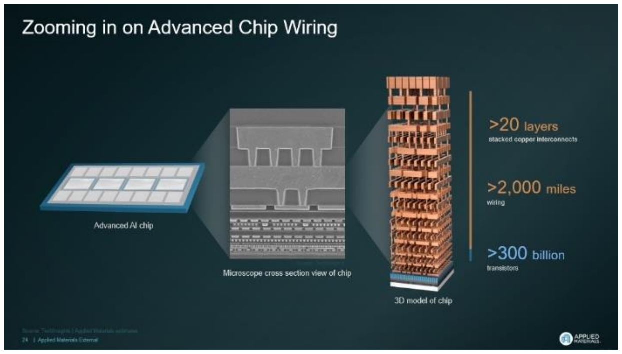
(Animation)

- Let's use an animation to highlight how the chip's wiring network is built.
- There are two key areas of the network.
- The first is the contact stack that connects the transistors to the rest of the chip's wiring.
- The second is the copper interconnect stack which contains all of the chip's signal and power wires.

- Each layer of the interconnect stack is built one layer at a time, with the horizontal lines connected by vertical vias.

- You'll notice that the wires are smallest near the transistors and that as we move further away from the transistors, the wires and vias become larger.

- The end result is a tall wiring network that is especially dense in the layers closest to the transistors and the source/drain regions Bala described.



Zooming in on Advanced Chip Wiring

>20 layers stacked copper interconnects

>2,000 miles wiring

>300 billion transistors

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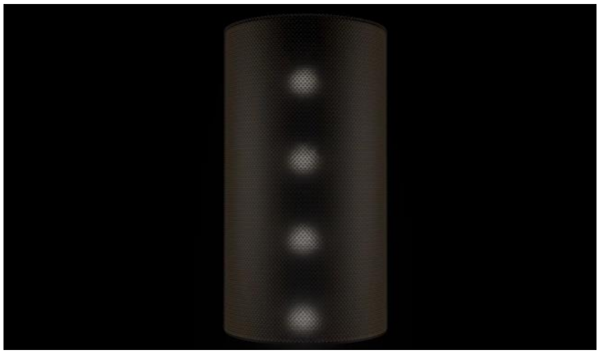
- To give you some perspective, leading-edge AI GPUs now in development will contain over 300 billion transistors and over 2,000 miles of wiring spread across more than 20 metal layers.

- In some chips, the wiring consumes just as much power as the transistors.

- So, to help improve system performance-per-watt, we need to innovate across the entire wiring stack, introducing new materials and new architectures.

- Now let's take a closer look at the contacts.



(Animation)

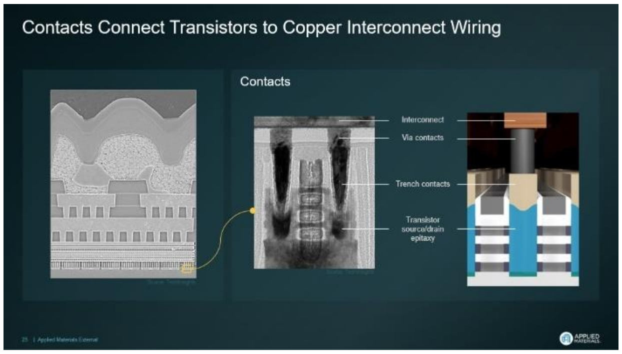
- Every signal that enters and exits the transistor passes through a contact.

- This tiny structure has an outsized impact on chip performance and energy efficiency.

- Picture a supercar stuck in bumper-to-bumper traffic—no matter how powerful the engine, the traffic jam limits the pace.

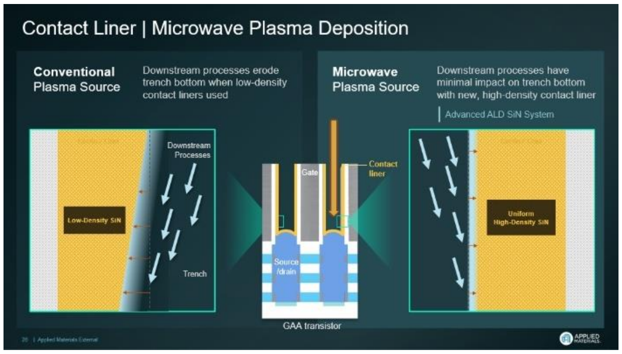
- In AI chips, the contact can easily become the traffic jam for electrons.

- It's such an intricate structure that very advanced materials engineering is needed to ensure the contact can keep up with modern AI workloads.



Contacts Connect Transistors to Copper Interconnect Wiring

- The contact begins at the source/drain trenches of the gate all around transistor, sitting on top of the source/drain epitaxy materials Bala described.
- Then the contact rises upward until it reaches the first, thinnest copper interconnect layer.
- The lower portion that touches the source/drain is called the trench contact, and the upper portion is called the via contact.
- Making a good contact without damaging the transistor requires building three key structures.



Contact Liner | Microwave Plasma Deposition

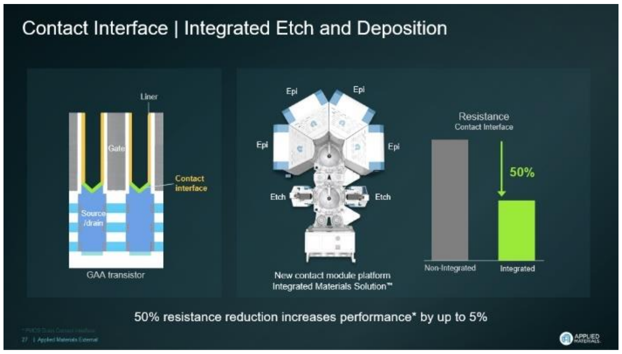
Conventional Plasma Source: Downstream processes erode trench bottom when low-density contact liners used

Microwave Plasma Source: Downstream processes have minimal impact on trench bottom with new, high-density contact liner

Advanced ALD SiN System

- The first is a protective contact liner that defines the dimensions of the contact wire and will later be filled with contact metal.
- Building a good liner is critical because later wiring process steps use aggressive process technologies that could distort the contact's shape.
- A contact liner made of chemically robust silicon nitride preserves the ideal shape throughout these downstream process steps.
- To protect the nearby transistor structures, the silicon nitride needs to be deposited at low temperature using a plasma-enhanced deposition process.
- But conventional plasma-enhanced deposition struggles to uniformly treat high-aspect-ratio structures such as the trench contact, leading to poor-quality silicon nitride films.
- To solve this issue, Applied has developed an advanced ALD silicon nitride liner system.
- In place of a conventional plasma source, the system uses an innovative, high-density microwave plasma which gently treats the silicon nitride within the tall, narrow structures.

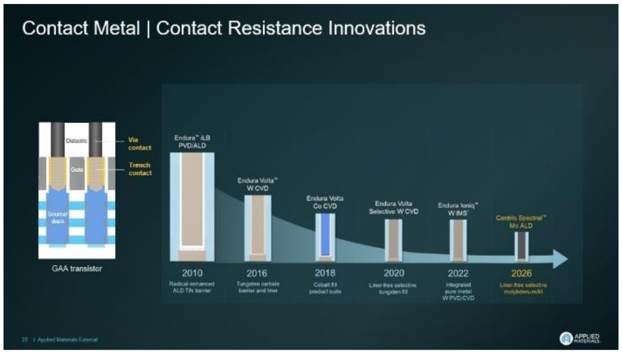
- The new system results in a dense, uniform silicon nitride film from the bottom of the contact trench to the top.
- With the protective contact liner in place, the next step should be depositing contact metal onto the source/drain epitaxy.
- Here, another challenge arises.



Contact Interface | Integrated Etch and Deposition

50% resistance reduction increases performance* by up to 5%

- Depositing metal directly onto the source/drain creates a mismatch of material properties at the materials boundary that increases contact resistance.
- To prevent this, we build a transition layer on top of the source/drain using a new system technology we plan to formally introduce in the near future.
- This special contact-module platform engineers the materials interface between the source/drain and the contact.
- This innovative product integrates Applied's advanced conductor etch and epitaxy technologies in one system—leading to another great example of the Integrated Materials System™ approach Kevin described earlier.
- The new system first etches a cavity into the source/drain epitaxy material that is precisely shaped to maximize surface area.
- Then, the same system uses epitaxy to deposit a special material that allows current to flow smoothly into the contact metal with minimal resistance.
- Our unique ability to integrate conductor etch and epitaxy in a single, high-vacuum system, allows us to reduce contact resistance by 50% as a compared to non-integrated approaches and help maximize the energy-efficient performance of the chip.


Contact Metal | Contact Resistance Innovations

- Once the new materials interface is formed, the trench is filled with metal to complete the lower portion of the contact.

- Then, the trench contact is extended as a via to connect to the first layer of the interconnect stack, and the via is filled with metal.

- For decades, tungsten was the industry’s contact metal of choice.

- Depositing the tungsten has been a two-step process.

- First, the contact liner is coated with a layer of material the bulk tungsten can adhere to.

- It’s like applying a thin coat of primer to a surface before applying a thicker coat of paint.

- But over time, as scaling reduced the size of the features, this thin coat of material consumed more of the volume, reducing the tungsten volume and increasing resistance.

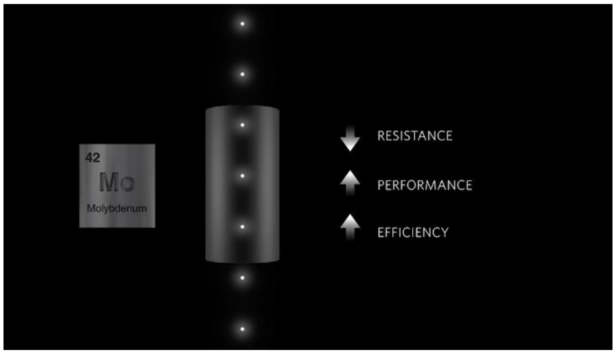
- To solve this problem, Applied developed a selective tungsten deposition process that enabled tungsten to be deposited directly into the contact trench.

- Today, as further scaling imposes even more space constraints, we need a new, lower-resistance metal.

- It is called molybdenum, or moly.

- Applied has decades of market leadership in selective materials deposition.

- Today, we’re extending our tungsten leadership in foundry-logic to moly using a new atomic layer deposition (ALD) system called Spectral™ Moly ALD.

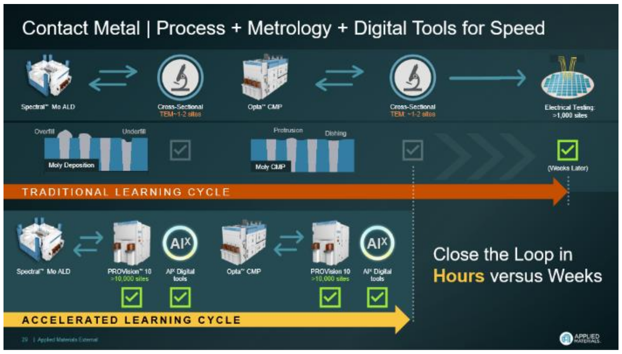


(Animation)

- This next-generation atomic layer deposition solution delivers atomic-level control for bottom-up, monocrystalline moly growth at sub-2nm GAA nodes.

- Spectral™ ALD reduces contact resistance by a further 15% as compared to selective tungsten in these smallest features, directly improving GAA chip performance while lowering power consumption.

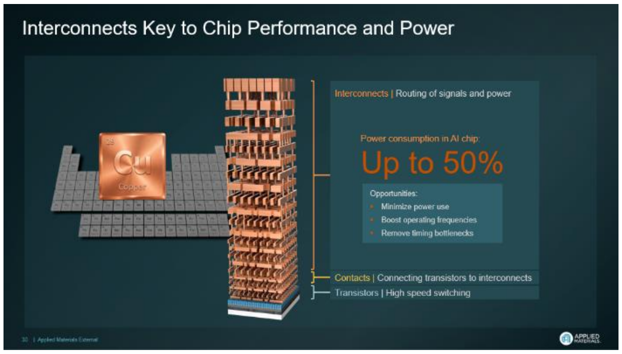
- In addition, we have co-optimized our new ALD moly technology with our chemical mechanical planarization (CMP) technology to ensure our customers achieve uniform, defect-free moly fill across the trillions of transistors on the wafer.


Contact Metal | Process + Metrology + Digital Tools for Speed

Close the Loop in **Hours** versus Weeks

- Specifically, our Opta™ CMP Platform has been co-optimized with the Spectral™ ALD system to help eliminate overfill, underfill, collapse and protrusions in the deposited moly.

- The other key ingredients to our cooptimized moly solution are Applied's PROVision™ 10 eBeam metrology system and our AI^{x}™ digital tools which provide rapid feedback on the deposition and planarization processes—shrinking the traditional process learning cycle from weeks to hours.


Interconnects Key to Chip Performance and Power

Interconnects | Routing of signals and power

Power consumption in AI chip:
Up to 50%

Opportunities:
- Minimize power use
- Boost operating frequencies
- Remove timing bottlenecks

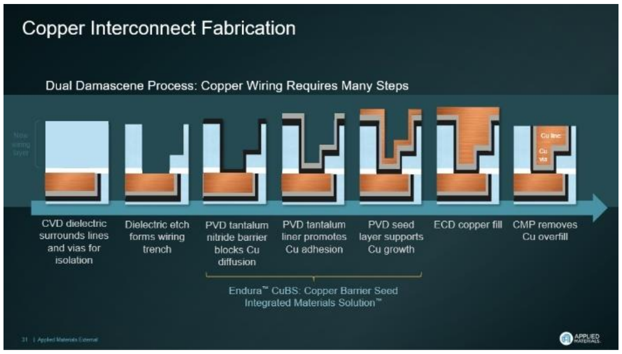
Contacts | Connecting transistors to interconnects

Transistors | High speed switching

- Now that the contact has been explained, let's talk about building the copper interconnect stack.

- Copper has been the interconnect metal of choice in the industry for nearly 30 years.

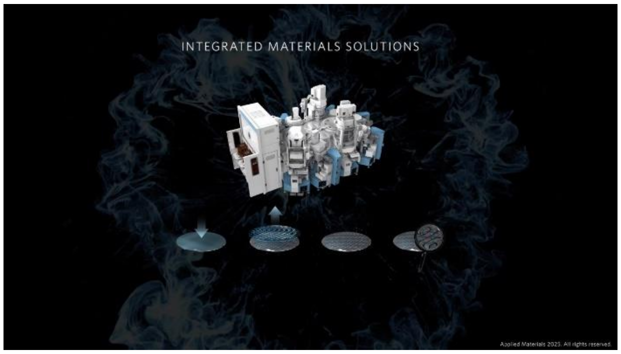
- Because copper is not etch-friendly, creating copper wires uses a process called dual damascene. I'll explain how it works.



Copper Interconnect Fabrication

Dual Damascene Process: Copper Wiring Requires Many Steps

- We begin making each layer of wiring by depositing insulating dielectric material across the wafer using chemical vapor deposition.
- The top of the layer is patterned, and etch is used to create features called trenches and vias in the dielectric layer that we will eventually fill with copper.
- Because copper can migrate and ruin chips if not well contained, it cannot be deposited into these features until they are first lined with a protective barrier made of tantalum nitride.
- Unfortunately, copper cannot be deposited directly on top of the tantalum nitride either because it fails to adhere to the surfaces and a poorly formed copper wire degrades performance, so we lay a pure tantalum liner on top of the barrier to improve copper adhesion and reliability.
- After the liner, we need to create a continuous seed layer of copper for the bulk fill that comes later.
- To achieve all these steps that make up modern copper wires, Applied many years ago developed a multi-step copper barrier seed process on the Endura™ platform that first precleans the incoming wafer, then deposits a tantalum nitride barrier, followed by a tantalum liner, and then a very thin layer of copper using physical vapor deposition (PVD)
- Once the copper barrier seed is in place, a simpler technology called copper electroplating (ECD) is used to fill the trenches with bulk copper.
- The ECD copper covers the entire wafer, and we use the term overburden to describe that the copper is now higher than the dielectric layer.
- A final step in completing the wiring layer is using chemical mechanical planarization—or CMP—to remove the copper until it is even with the top of the dielectric layer.
- From this perfectly uniform surface, the next layer of metal can be created, sometimes using the very same process sequence.
- To this day, copper barrier seed on the Endura™ platform is one of Applied's largest businesses, and Applied is #1 in PVD and CVD—both overall, and in on-chip wiring and advanced packaging applications.



INTEGRATED MATERIALS SOLUTIONS

(Animation)

- A key attribute of the Endura™ system is that it creates and maintains an extraordinarily high vacuum.
- This vacuum keeps wafers protected from the cleanroom atmosphere which is full of impurities that can contaminate metals and degrade chip performance, reliability and yield.
- Over time, Applied has added many technologies beyond PVD to the Endura™ platform, including CVD, ALD, more advanced precleans, thermal processes and other materials modification treatments.
- This makes Endura the workhorse for our integrated materials systems, used when wafers need to stay in a pristine, high-vacuum environment as multiple consecutive processes are performed, as we'll soon discuss.
- Next, let's discuss the CVD dielectric materials I described a moment ago.

Reducing Wiring Capacitance | Low-k Dielectrics

Challenges

Reducing Capacitance with More Porous, Lower-k Dielectrics

Maintaining Mechanical Strength of Lower-k Dielectric Films

Producer™ Black Diamond™ PECVD

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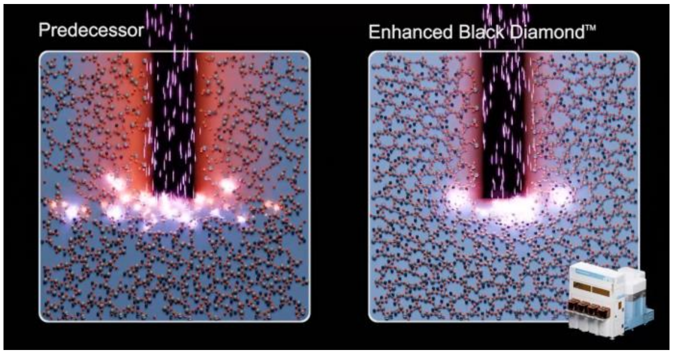
- As wiring density increases and the copper wiring layers scale and become closer together, parasitic capacitance increases.
- The dielectric materials need to be engineered to reduce this capacitance, and they do this with porosity, adding tiny air pockets which are excellent insulators.
- We call these films "low-k." They ensure low-capacitance, and they are essential to fast signaling.
- Applied's Black Diamond™ low-k dielectric has become very successful in the industry and a key reason why Applied is #1 in CVD overall, as well as in on-chip wiring and advanced packaging applications.
- As wiring layers become thinner, the porosity of low-k films becomes an issue because the materials are mechanically weaker than the surrounding metals.
- At the higher wiring levels, the mechanical issue is manageable because the films are thick enough to remain robust.

- But as the industry transitions to 2nm gate-all-around and beyond, the dielectric layers nearest the transistors become extremely thin.

- There is an increasing risk of film cracking and collapse which creates chip yield and reliability issues.



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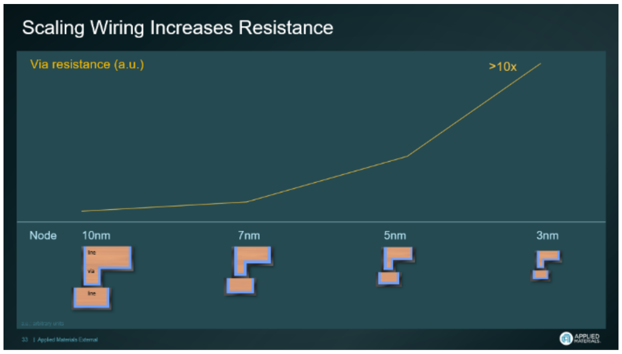
- To address this problem, Applied has developed Enhanced Black Diamond™, a new dielectric material.

- Enhanced Black Diamond™ has a stronger chemical bonding network that increases mechanical strength by 40% which enables gate all around wiring layer scaling in the 2nm node and beyond.

- Next let's return to the wiring, which in the upper layers is about depositing a PVD tantalum nitride barrier, tantalum liner, PVD copper seed, and bulk copper, then polishing the copper wires with CMP.



Scaling Wiring Increases Resistance

a.u.: arbitrary units

- However, over the generations of logic scaling Bala described, the wiring has scaled along with the transistors to smaller dimensions, and resistance has increased.

- The resistance is most problematic in the vertical via structures that interconnect the horizontal wiring layers.

- To keep the wiring from consuming most of the chip's power, Applied has continuously developed new materials innovations for vias—which I'll now describe.

- There are two key challenges.

Reducing Resistance | Selective ALD Barrier

Challenge

Standard barrier integration

Via resistance increases up to 100% from 5nm to 3nm node

Selective ALD barrier integration

Eliminating barrier at bottom enables low-resistance copper-to-copper contact

Up to 50% lower via resistance compared to standard barrier

- Copper Reflow
- Liner Deposition
- Materials Modification Treatment
- Integrated On-Board Metrology
- Selective ALD Deposition
- Interface Engineering
- Surface Preparation

Endura™ CuBS™ IMS™

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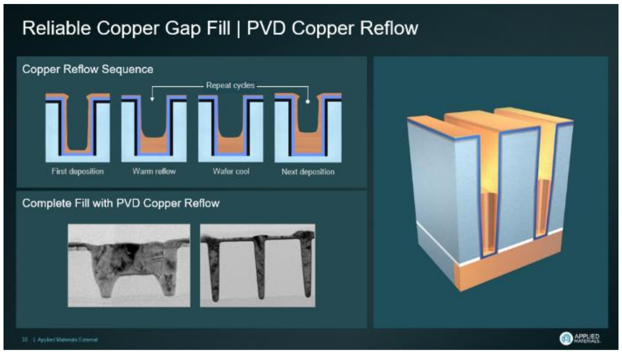
- First, as the wiring scales, the barrier and liner take up an increasing percentage of the space available for copper—driving up resistance.
- Second, where the barrier meets copper on the layer below, resistance also builds.
- As a result, much of the materials engineering breakthroughs that have extended copper wiring focus on new, increasingly thinner liner barriers and new ways of depositing copper into the very smallest trenches.
- One of the best examples of this is Applied's Endura™ Copper Barrier Seed (CuBS) IMS™ or Integrated Materials System™.
- This Endura™ system combines seven different process technologies in high vacuum, including ALD, PVD, CVD, copper reflow, surface treatment, materials interface engineering and metrology.
- In this IMS™ solution, the conformal ALD barrier is replaced with a selective ALD barrier that eliminates the high-resistivity tantalum nitride barrier from the bottom of the vias.
- The process provides a pure, conductive, metal-to-metal path for electrons to flow from one metal layer to the next.
- The system also replaces both copper seed and copper electroplating in targeted layers with a process called copper reflow.



Reliable Copper Gap Fill | PVD Copper Reflow

Copper Reflow Sequence

Complete Fill with PVD Copper Reflow

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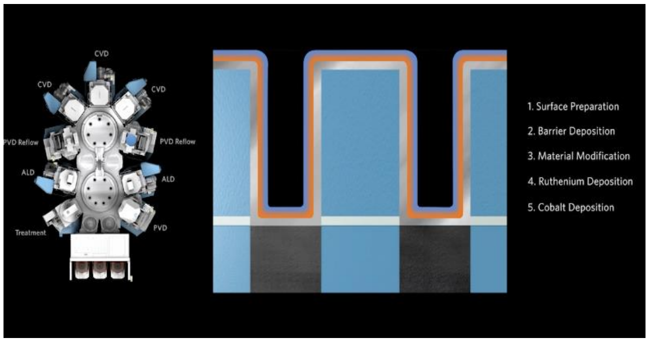
- In copper reflow, a sequence of copper deposition and gentle heat steps slowly fills the narrow vias with void-free copper.
- As a result, electrical resistance at the via contact interface is reduced by up to 50%, improving chip performance and power consumption, and enabling logic scaling at the 3nm logic node and beyond.



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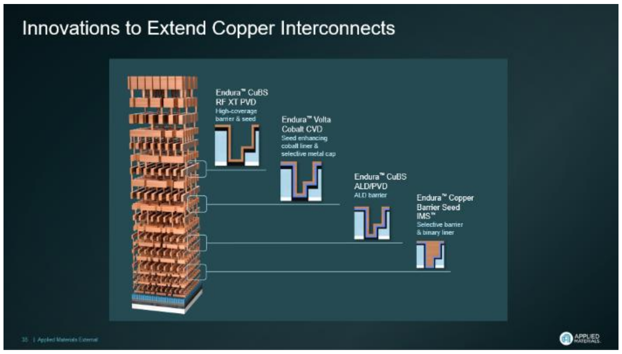
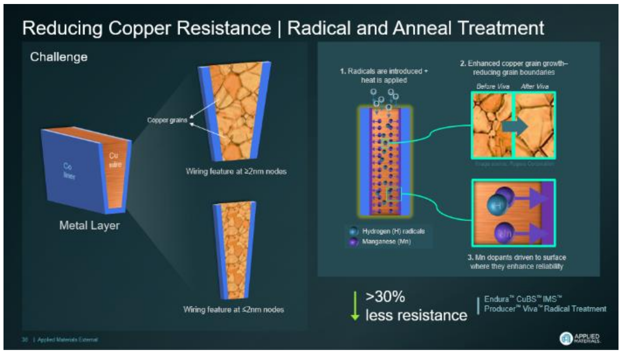
- Applied also added the industry’s first binary liner to the Endura™ IMS™ system.
- We combine ruthenium and cobalt atoms to build a new liner that is around 33% thinner than the previous best.
- Our new RuCo liner creates more room for copper metal—which in turn reduces wiring resistance and heat, boosting chip performance per watt at the 2nm node and below.
- Today’s advanced logic chips combine a number of these wiring technologies.



Innovations to Extend Copper Interconnects

- We continue to use the earlier technologies in the taller layers of the stack and insert the newer technologies in the tighter layers of the middle and bottom of the stack, which ultimately connects to the tungsten and moly transistor contacts we discussed earlier.
- In the bottom layers, Enhanced Black Diamond™ has been co-optimized to work with our latest Endura™ Copper Barrier Seed (CuBS) IMS™ systems.
- This layer-optimized approach allows Applied to support the entire wiring stack with an optimized solution for every level.
- Nearly every chip produced over the past 30 years has relied on an Endura™ system.
- Copper remains the workhorse of the overall chip wiring market.
- As we look three generations ahead into the next decade of the industry’s future, we see further extensions to copper wiring based on new Endura™ systems combining PVD, ALD, CVD, copper reflow and other technologies into a single system.
- Wiring innovation leadership such as what I’ve just described is a major reason why Applied derives around 30% of its business from Integrated Materials Solutions™.

- Earlier we talked about a large and important equipment market called materials modification, which includes treatments.
- As we continue to scale, treatments are playing an important role in wiring as well, which I'll now explain.



Reducing Copper Resistance | Radical and Anneal Treatment

Challenge

Metal Layer

Copper grains

Wiring feature at ≥2nm nodes

Wiring feature at ≤2nm nodes

1. Radicals are introduced + heat is applied

2. Enhanced copper grain growth–reducing grain boundaries

Before Viva

After Viva

Hydrogen (H) radicals

Manganese (Mn)

3. Mn dopants driven to surface where they enhance reliability

>30% less resistance

Endura™ CuBS™ IMS™
Producer™ Viva™ Radical Treatment

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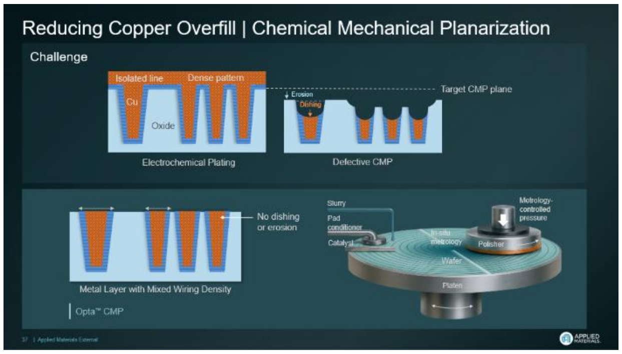
- An important thing to appreciate is that copper can be made up of many tiny crystal grains.
- The areas where the grains meet are called grain boundaries, and in these regions, electrons can scatter, causing them to slow down.
- You might think of the grain boundaries as speed bumps for electrons that get more problematic with scaling, increasing resistance.
- In addition, as the copper wires become thinner with scaling, dopants such as manganese are often used to improve their reliability.
- To help our customers, Applied has developed an innovative treatment solution that is co-optimized with the Endura™ system's copper deposition.
- Immediately after deposition, we treat the metal to ensure optimal performance.
- In fact, this is a new wiring application of the Producer™ Viva™ treatment system Bala mentioned earlier, used to smooth the silicon channels in GAA transistors.
- Viva™ uses hydrogen radicals to help the copper crystals grow larger, which results in fewer grain boundaries and even lower resistance.
- The hydrogen radicals also help move the manganese to the surface, which is exactly where we need them to be to increase reliability—instead of deeper within the copper wiring where they add resistance.
- The Viva™ treatment also applies a thermal anneal, using carefully controlled heat to further enhance manganese segregation as well as boost copper grain growth to reduce grain boundary scattering sites.
- The Viva™ treatment co-optimized with Endura™ can reduce copper wiring resistance by over 30%—leading to meaningful improvements in overall chip performance.



Reducing Copper Overfill | Chemical Mechanical Planarization

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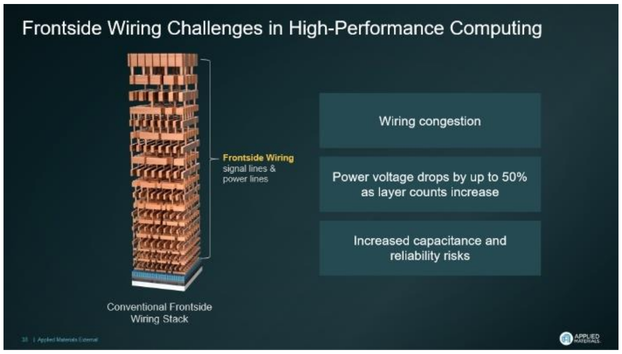
- Once the copper metallization is optimized, we use chemical mechanical planarization—or CMP—to make sure every wiring layer is perfectly uniform with the surrounding dielectrics.
- Earlier, Kevin mentioned that lowering variability is a critical lever for improving performance-per-watt in wiring.
- This variability can be pronounced today as chip designs integrate many different wiring sizes and densities on the same layers.
- These designs make copper CMP increasingly challenging because different types of wiring polish at different rates.
- To manage this complexity, Applied has developed innovative copper CMP processes on the Opta™ CMP platform, designed to planarize all of the wiring in each layer with nanometer precision.
- Opta™ CMP accomplishes this by applying advanced zone and pressure control that dynamically adjusts the polishing process to compensate for these pattern-density differences.
- The result is an exceptionally flat, uniform surface—which is extremely critical for EUV lithography, where the limited depth of focus makes even small surface variations a yield risk.
- Innovations like Opta™ are why Applied has the #1 share position in CMP overall and particularly in advanced applications.
- My final topic today is backside wiring.
- Applied's frontside wiring innovations in transistor contacts, dielectric materials, protective liner barriers, copper barrier seed and copper reflow are being ported to backside wiring applications as well.



Frontside Wiring Challenges in High-Performance Computing

Wiring congestion

Power voltage drops by up to 50% as layer counts increase

Increased capacitance and reliability risks

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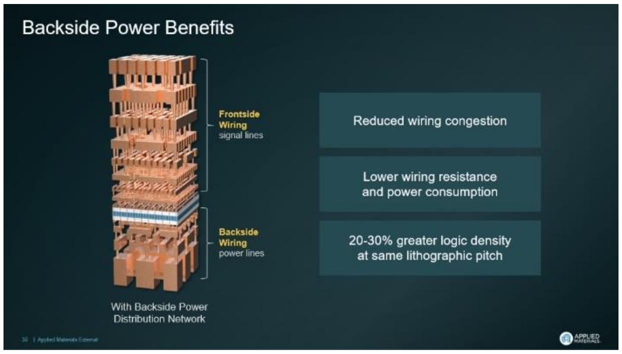
- Frontside wiring is becoming most challenging in high-performance computing where the largest number of gate-all-around transistors are being packed into the largest possible die sizes, creating the need for even taller wiring stacks.

- Power lines and signal wires are both combined in frontside networks, creating congestion and capacitance which reduces chip performance per watt.

- As the number of frontside wiring layers increases, voltage drops by as much as 50%, increasing the risk of chip reliability issues.

- In addition, including the thick power lines in the logic cell makes it more difficult to scale logic designs to the smallest possible dimensions.



Backside Power Benefits

With Backside Power Distribution Network

Reduced wiring congestion

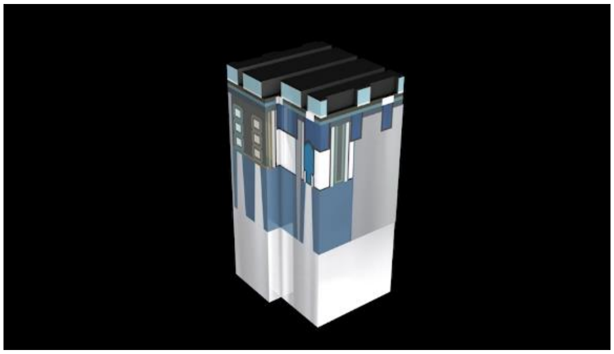
Lower wiring resistance and power consumption

20-30% greater logic density at same lithographic pitch

- To relieve this bottleneck, the industry is developing logic nodes with backside power.

- This is another example of the DTCO innovations that Bala mentioned earlier.

- The benefits of backside wiring include frontside wiring design simplicity, higher chip performance, lower wiring resistance and power consumption, and tighter logic cell integration which can increase logic density by as much as 20-30% at the same lithography.



(Animation)

- I hope you now have a good understanding of how the transistor innovations Bala discussed are increasing wiring complexities that we are putting equal energy into solving for our customers.

- After all, the best transistors in the world can’t live up to their potential unless the wiring is just as innovative.

- Together, Applied’s transistor and wiring technologies are the foundation of better computing performance per watt.

- And as Bala mentioned earlier, the logic roadmap innovations you've learned about today are becoming increasingly important in DRAM as well, and this applies both to transistors and wiring.
- We'll have more to say about that in the DRAM and Advanced Packaging Master Class.

MASTER CLASS April 8, 2026

Event Summary and EPIC Preview

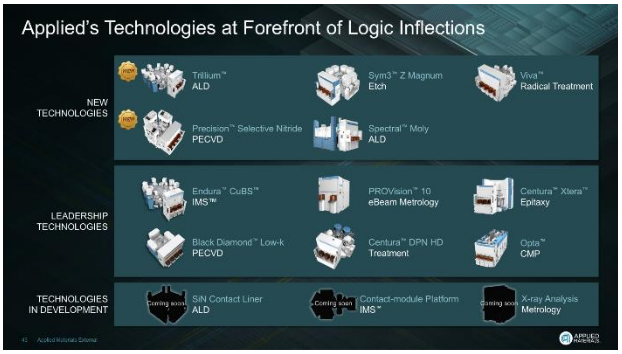
Kevin Moraes, Ph.D.
Corporate Vice President
Strategy and Marketing
Semiconductor Products Group

- Thank you, Zhebo and Bala, for taking us through the transistor and wiring inflections that are enabling next-generation logic chips that will be soon be available in the marketplace.

KEY
MESSAGES

- AI is driving unprecedented demand for semiconductors and wafer fab equipment
- Fastest growing areas of the WFE market are leading-edge foundry-logic, DRAM including HBM, and Advanced Packaging, where Applied has strong leadership
- Materials engineering is increasingly key to roadmap inflections
- Applied is ramping innovations that enable new transistors and wiring for energy-efficient AI
- Inflection-focused innovation creates shared value for customers and Applied

- For nearly six decades, Applied Materials has played a foundational role in driving the semiconductor industry roadmap, and there's never been a more exciting time for us.
- The era of simple 2D scaling with a limited set of materials is over.
- The next decade will be driven by new materials, new 3D device architectures, and advanced packaging—connecting more chiplets to maximize logic density, memory, and I/O in a single product.
- This is where the industry is headed—and where Applied has a leadership role to play.



Applied's Technologies at Forefront of Logic Inflections

NEW TECHNOLOGIES
Trillium™ ALD
Sym3™ Z Magnum Etch
Viva™ Radical Treatment
Precision™ Selective Nitride PECVD
Spectral™ Moly ALD

LEADERSHIP TECHNOLOGIES
Endura™ CuBS™ IMS™
PROVision™ 10 eBeam Metrology
Centura™ Xtera™ Epitaxy
Black Diamond™ Low-k PECVD
Centura™ DPN HD Treatment
Opta™ CMP

TECHNOLOGIES IN DEVELOPMENT
SiN Contact Liner ALD
Contact-module Platform IMS™
X-ray Analysis Metrology

- Applied Materials has the industry's broadest portfolio of technologies for this future, and we will soon open the EPIC Center in Silicon Valley where we will drive co-innovation of these advances with our customers.

Complexity: Innovation to Commercialization Timeline

Can Take **10-15 YEARS** Today!

- New **materials**
- New **processes**
- More **step-to-step interactions**

- New **interactions**
- New **selective processes**

- New **technologies**
- More **interfaces**

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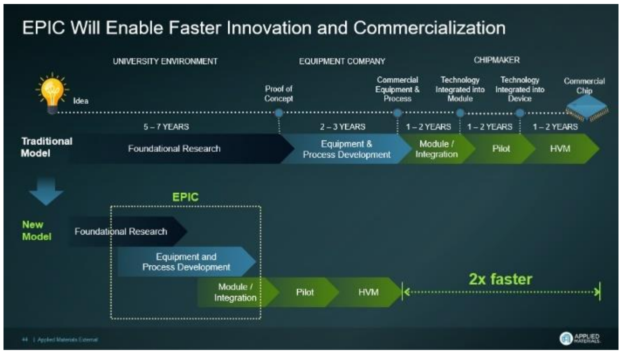
- Some of the breakthrough materials and techniques you learned about in today's Master Class took as many as 15 years to develop, from ideation to commercialization.
- But the energy constraints facing the AI ecosystem demand a much faster pace.
- With EPIC—which stands for Equipment and Process Innovation and Commercialization—we are building a secure environment where our top innovators can co-innovate with their counterparts from our customers, partners, and top academic institutions.
- The EPIC Center will take years off the traditional, serial innovation model.



EPIC Will Enable Faster Innovation and Commercialization

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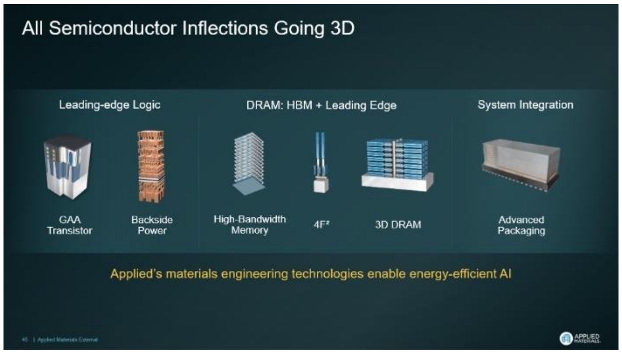
- It will be the only place in the world where our customers can have first access to the materials and process technologies that will enable new semiconductor architectures for AI.



All Semiconductor Inflections Going 3D

Applied's materials engineering technologies enable energy-efficient AI

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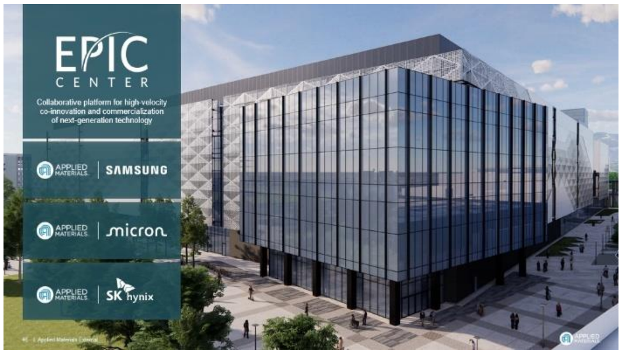
- We will develop leading-edge logic technologies including future gate all around transistors and CFETs that will process data faster and with lower power.

- We will develop new memory technologies including 3D DRAM.

- And we will pioneer new packaging innovations including high-bandwidth memory chip stacking with hybrid bonding.

- At the EPIC Center, we will work three nodes and more than a decade into the future, giving our customers first access to unique materials, process recipes and hardware innovations.



EPIC CENTER

Collaborative platform for high-velocity co-innovation and commercialization of next-generation technology

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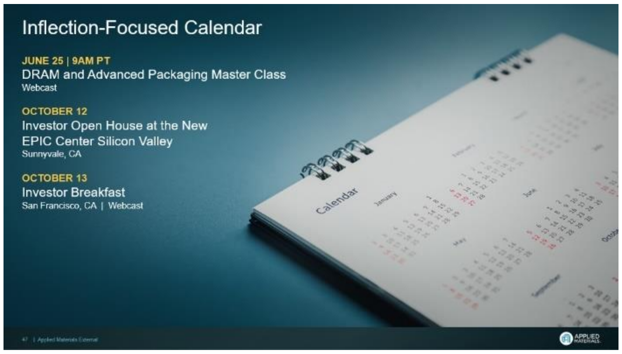
- We will co-innovate together and then transfer these innovations to our customers' R&D labs to be integrated into their future products more rapidly than ever before, accelerating hardware progress throughout the entire technology ecosystem.



Inflection-Focused Calendar

JUNE 25 | 9AM PT
DRAM and Advanced Packaging Master Class
Webcast

OCTOBER 12
Investor Open House at the New
EPIC Center Silicon Valley
Sunnyvale, CA

OCTOBER 13
Investor Breakfast
San Francisco, CA | Webcast

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- We hope you enjoyed today's master class, and we hope you'll join us in June for our DRAM and Advanced Packaging class.

APPLIED MATERIALS™
Material Innovation