Applied Materials Unveils Chip Wiring Innovations for More Energy-Efficient Computing

July 8, 2024

- *Industry's first use of ruthenium in high-volume production enables copper chip wiring to be scaled to the 2nm node and beyond and reduces resistance by as much as 25%*
- *New enhanced low-k dielectric material reduces chip capacitance and strengthens logic and DRAM chips for 3D stacking*

SANTA CLARA, Calif., July 08, 2024 (GLOBE NEWSWIRE) -- Applied Materials, Inc. today introduced materials engineering innovations designed to increase the performance-per-watt of computer systems by enabling copper wiring to scale to the 2nm logic node and beyond.

"The AI era needs more energy-efficient computing, and chip wiring and stacking are critical to performance and power consumption," said Dr. Prabu Raja, President of the Semiconductor Products Group at Applied Materials. "Applied's newest integrated materials solution enables the industry to scale low-resistance copper wiring to the emerging angstrom nodes, while our latest low-k dielectric material simultaneously reduces capacitance and strengthens chips to take 3D stacking to new heights."

Overcoming the Physics Challenges of Classic Moore's Law Scaling

Today's most advanced logic chips can contain tens of billions of transistors connected by more than 60 miles of microscopic copper wiring. Each layer of a chip's wiring begins with a thin film of dielectric material, which is etched to create channels that are filled with copper. Low-k dielectrics and copper have been the industry's workhorse wiring combination for decades, allowing chipmakers to deliver improvements in scaling, performance and power-efficiency with each generation.

However, as the industry scales to 2nm and below, thinner dielectric material renders chips mechanically weaker, and narrowing the copper wires creates steep increases in electrical resistance that can reduce chip performance and increase power consumption.

Enhanced Low-k Dielectric Reduces Interconnect Resistance and Strengthens Chips for 3D Stacking

Applied's Black Diamond™ material has led the industry for decades, surrounding copper wires with a low-dielectric-constant – or "k-value" – film engineered to reduce the buildup of electrical charges that increase power consumption and cause interference between electrical signals.

Applied today introduced an enhanced version of Black Diamond, the latest in the company's Producer™ Black Diamond™ PECVD family. This new material reduces the minimum k-value to enable scaling to 2nm and below, while offering increased mechanical strength which is becoming critical as chipmakers and systems companies take 3D logic and memory stacking to new heights.

The latest Black Diamond technology is being adopted by all leading logic and DRAM chipmakers.

New Binary Metal Liner Enables Ultrathin Copper Wires

To scale chip wiring, chipmakers etch each layer of low-k film to create trenches, then deposit a barrier layer that prevents copper from migrating into the chip and creating yield issues. The barrier is then coated with a liner that ensures adhesion during the final copper reflow deposition sequence, which slowly fills the remaining volume with copper.

As chipmakers further scale the wiring, the barrier and liner take up a larger percentage of the volume intended for wiring, and it becomes physically impossible to create low-resistance, void-free copper wiring in the remaining space.

Today, Applied Materials publicly introduced its latest IMS™ (Integrated Materials Solution™) which combines six different technologies in one high-vacuum system, including an industry-first combination of materials that enables chipmakers to scale copper wiring to the 2nm node and beyond. The solution is a binary metal combination of ruthenium and cobalt (RuCo), which simultaneously reduces the thickness of the liner by 33 percent to 2nm, produces better surface properties for void-free copper reflow, and reduces electrical line resistance by up to 25 percent to improve chip performance and power consumption.

The new Applied Endura™ Copper Barrier Seed IMS™ with Volta™ Ruthenium CVD* is being adopted by all leading logic chipmakers and bega shipping to customers at the 3nm node. An animation of the technology can be viewed here.

Customer Comments

"While advances in patterning are driving continued device scaling, critical challenges remain in other areas including interconnect wiring resistance, capacitance and reliability," said Sunjung Kim, VP & Head of Foundry Development Team at Samsung Electronics. "To help overcome these challenges, Samsung is adopting multiple materials engineering innovations that extend the benefits of scaling to the most advanced nodes."

"The semiconductor industry must deliver dramatic improvements in energy-efficient performance to enable sustainable growth in AI computing," said Dr. Y.J. Mii, Executive Vice President and Co-Chief Operating Officer at TSMC. "New materials that reduce interconnect resistance will play an important role in the semiconductor industry, alongside other innovations to improve overall system performance and power."

A Growing Wiring Opportunity

Applied is the industry leader in chip wiring process technologies. From the 7nm node to the 3nm node, interconnect wiring steps have approximately tripled, increasing Applied's served available market opportunity in wiring by more than $1 billion per 100,000 wafer starts per month (100K WSPM) of greenfield capacity, to approximately $6 billion. Looking ahead, the introduction of backside power delivery is expected to increase Applied's wiring opportunity by another $1 billion per 100K WSPM, to approximately $7 billion.

The new chip wiring products, along with other materials engineering innovations for making future AI chips, will be discussed at Applied's SEMICON West 2024 Technology Breakfast. The presentation and other materials from the event will be available on the Applied Materials website at: https://ir.appliedmaterials.com on Tuesday, July 9, 2024 at approximately 9:00 a.m. ET / 6:00 a.m. PT.

*PECVD = Plasma-Enhanced Chemical Vapor Deposition
*CVD = Chemical Vapor Deposition

Forward-Looking Statements
This press release contains forward-looking statements, including those regarding anticipated benefits of our new products and technologies, expected growth and trends in our businesses and markets, industry outlooks and demand drivers, technology transitions, and other statements that are not historical facts. These statements and their underlying assumptions are subject to risks and uncertainties and are not guarantees of future performance. Factors that could cause actual results to differ materially from those expressed or implied by such statements include, without limitation: failure to realize anticipated benefits of our new products and technologies; the level of demand for semiconductors and for our products and technologies; customers' technology and capacity requirements; the introduction of new and innovative technologies, and the timing of technology transitions; market acceptance of existing and newly developed products; the ability to obtain and protect intellectual property rights in technologies; our ability to ensure compliance with applicable law, rules and regulations; and other risks and uncertainties described in our SEC filings, including our recent Forms 10-Q and 8-K. All forward-looking statements are based on management's current estimates, projections and assumptions, and we assume no obligation to update them.

About Applied Materials
Applied Materials, Inc. (Nasdaq: AMAT) is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible a better future. Learn more at www.appliedmaterials.com.

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Photos accompanying this announcement are available at

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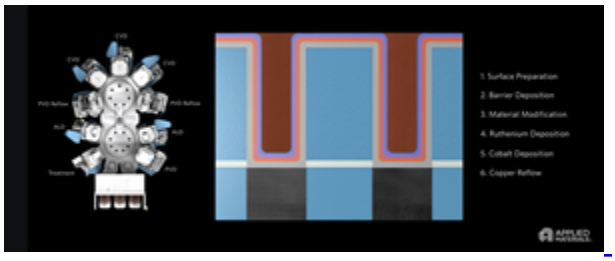
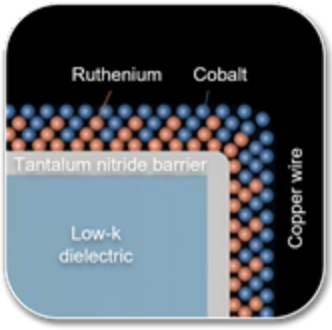
Applied Materials' Latest Integrated Materials Solution™ Extends Copper Wiring to 2nm and Beyond



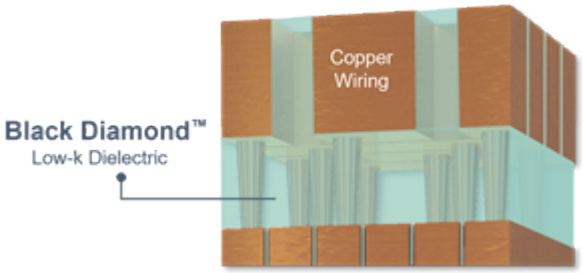
Applied Materials' new Endura™ Copper Barrier Seed IMS™ with Volta™ Ruthenium CVD combines six different technologies in one high-vacuum system, including an industry-first combination of materials that enables chipmakers to scale copper wiring to the 2nm node and beyond.

Combining Ruthenium and Cobalt Improves Chip Performance and Power Consumption



With the semiconductor industry's first use of ruthenium in high-volume production, Applied Materials' new binary metal combination of ruthenium and cobalt (RuCo) enables copper chip wiring to be scaled to the 2nm node and beyond and reduces electrical line resistance by as much as 25 percent.

Enhanced Black Diamond™ Reduces Interconnect Resistance and Strengthens Chips for 3D Stacking



Applied Materials today introduced an enhanced version of the company's Producer™ Black Diamond™ PECVD dielectric film. This new material enables chip scaling to 2nm and below, while offering increased mechanical strength to help take 3D logic and memory stacking to new heights.

Source: Applied Materials, Inc.